TPS65950

Integrated Power Management/Audio Codec

Silicon Revision 1.2

Data Manual

Literature Number: SWCS032E

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Integrated Power Management/Audio Codec

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1 Introduction

The TPS65950 device is a highly integrated power-management and audio coder/decoder (codec) integrated circuit (IC) that supports the power and peripheral requirements of the OMAP™ application processors. The device contains power management, an audio codec, a universal serial bus (USB) high-speed (HS) transceiver, an ac/USB charger, light-emitting diode (LED) drivers, an analog-to-digital converter (ADC), a real-time clock (RTC), and embedded power control.

The power portion of the device contains three buck converters, two controllable by a dedicated SmartReflex™ class-3 interface, multiple low-dropout (LDO) regulators, an embedded power controller (EPC) to manage the power-sequencing requirements of OMAP, and an RTC and backup module. The RTC can be powered by a backup battery when the main supply is not present, and the device contains a coin-cell charger to recharge the backup battery as needed.

The USB module provides a HS 2.0 on-the-go (OTG) transceiver suitable for direct connection to the OMAP universal transceiver macrocell interface (UTMI) + low pin interface (ULPI) with an integrated charge pump (CP) and full support for the carkit Consumer Electronics Association (CEA)-936A specification.

The Li-ion battery charger supports charging from ac chargers, USB host devices, USB chargers, or carkits. The type of charger is detected automatically by the device, which provides hardware-controlled linear charging with ac chargers, USB chargers, and carkits, in addition to software-controlled charging for all charger types.

The audio codec in the device includes five digital-to-analog converters (DACs) and two ADCs to provide multiple voice channels and stereo downlink channels that can support all standard audio sample rates through several inter-IC sound (I2S™)/time division multiplexing (TDM) format interfaces. The audio output stages on the device include stereo headset amplifiers, two integrated class-D amplifiers providing stereo differential outputs, predrivers for line outputs, and an earpiece amplifier. The input audio stages include three differential microphone inputs, stereo line inputs, and interface for digital micrphones. Automatic and programmable gain control is available with all necessary digital filtering, side-tone functions, and pop-noise reduction.

The device also provides a auxiliary modules, including LED drivers, and ADC, keypad interface, and general-purpose inputs/outputs (GPIOs). The LED driver can power two LED circuits to illuminate a panel or provide user indicators. The drivers also provide pulse width modulation (PWM) circuits to control the illumination levels of the LEDs. The ADC monitors signals entering the device, such as supply and charging voltages, and has multiple additional external ADC inputs for system use. The keypad interface implements a built-in scanning algorithm to decode hardware-based key presses and to reduce software use, with multiple additional GPIOs that can be used as interrupts when they are configured as inputs.

This TPS65950 Data Manual describes the electrical and mechanical specifications for the TPS65950. It covers the following topics:

- TPS65950 terminals: Assignment, multiplexing, electrical characteristics, and functional description (see Section 2, *Terminal Description*)
- Electrical characteristic requirements: Maximum and recommended operating conditions, digital input/output (I/O) characteristics (see Section 3, *Electrical Characteristics*)
- Power module, including the power provider, power references, power control, power consumption, and power management with the on and off sequences (see Section 4, *Power Module*)
- RTC and EPC (see Section 5, *Real-Time Clock and Embedded Power Controller*)
- Audio/voice module with the electrical characteristics and the application schematics for the downlink and uplink paths (see Section 6, *Audio/Voice Module*)

- Battery charger interface (see Section 8, *Battery Interface*)
- Various modules: Monitoring analog-to-digital conversion (MADC), LED drivers, and keyboard (see Section 9, *MADC*, Section 10, *LED Drivers*, and Section 11, *Keyboard*)
- Clock specifications: Clock slicer, input and output clocks (see Section 12, *Clock Specifications*)
- Timing requirements and switching characteristics (ac timings) of the interfaces (see Section 13, *Timing Requirements and Switching Characteristics*)
- Deboucing time (see Section 14, *Debouncing Time*)
- External components for the application schematics (see Section 15, *External Components*)
- Thermal resistance characteristics, device nomenclature, and mechanical data about the available packaging (see Section 16, *TPS65950 Package*)
- Glossary of acronyms and abbreviations used in this data manual (see Section 17, *Glossary*)

1.1 Features

- **Power:**
  - **Three efficient stepdown converters**
    - **VDD1: TPS65950A2 with 1.2A and TPS65950A3 with 1.4A (for 1GHz speed)**
    - **VDD2: 600mA**
    - **VIO: 700mA**
  - **10 external linear LDOs for clocks and peripherals**
  - **SmartReflex dynamic voltage management**
- **Audio:**
  - **Voice codec**
  - **15-bit linear codec (8 and 16 kHz)**
  - **Differential input main and submicrophones**
  - **Differential headset microphone input**
  - **Auxiliary/FM input (mono or stereo)**
  - **Differential 32-Ω speaker and 16-Ω headset drivers (external predrivers for class D)**
  - **8-Ω stereo class-D drivers**
  - **Pulse code modulation (PCM) and TDM interfaces**
  - **Bluetooth® interface**
  - **Automatic level control (ALC)**
  - **Digital and analog mixing**
  - **16-bit linear audio stereo DAC (96, 48, 44.1, and 32 kHz, and derivatives)**
  - **16-bit linear audio stereo ADC (48, 44.1, and 32 kHz, and derivatives)**
  - **Digital microphone inputs**
  - **Carkit**
- **Charger:**
  - **Li-ion, Li-on polymer, and cobalt-nickel-manganese charger**
  - **Supports charging with ac-regulated charger (maximum 7 V), USB host devices, Mobile Computing Promotion Consortium (MCPC) devices, USB chargers, and carkit chargers (maximum 7 V)**
  - **Backup battery charger**
- **USB:**
  - **USB 2.0 OTG-compliant HS transceivers**
  - **12-bit ULPI**
  - **USB power supply (5-V CP for VBUS)**
  - **CEA-2011: OTG transceiver interface specification**
  - **CEA-936A: Mini-USB analog carkit interface specification**
  - **MCPC ME-universal asynchronous receiver/transmitter (UART) GL-006 specification**
- **Additional features:**
  - **LED driver circuit for two external LEDs**
  - **10-bit MADC with 3 to 8 external inputs**
  - **RTC and retention modules**
  - **HS inter-integrated circuit (I^2C™) serial control**
  - **Thermal shutdown and hot-die detection**
  - **Keypad interface (up to 8 × 8)**
  - **External vibrator (vibrator) control**
  - **19 GPIO devices**
  - **0.4-mm pitch, 209 pin, 7 × 7 mm package**

1.2 TPS65950 Block Diagram

Figure 1-1 is a block diagram of the TPS65950.

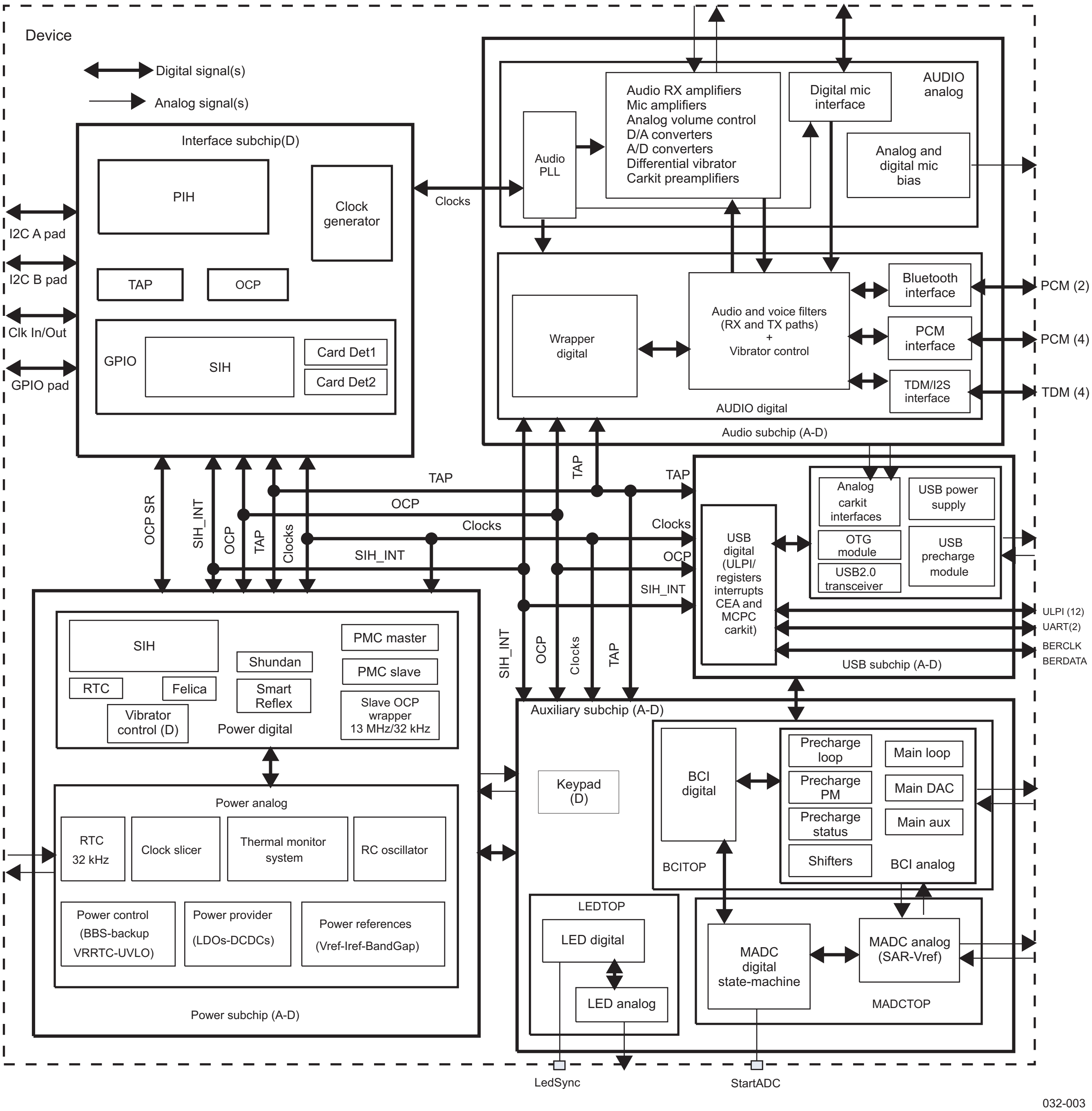


Figure 1-1. TPS65950 Block Diagram

2 Terminal Description

Figure 2-1 shows the ball locations for the 209-ball plastic ball grid array (PBGA) package and is used with Table 2-1 to locate signal names and ball grid numbers.

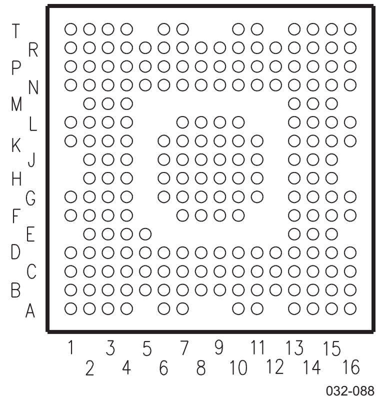


Figure 2-1. PBGA Bottom View

2.1 Corner Balls

The four corner balls (see the following list) are not usable for functional pins:

- Test
- TestV1
- Test.RESET
- TestV2

The eight corner adjacent balls are:

- RFID.EN
- UART1.TXD
- JTAG.TDI/BERDATA
- JTAG.CLK/BERCLK
- PCM.VFS
- PCM.VDX
- PCM.VDR
- PCM.VCK

2.2 Ball Characteristics

Table 2-1 describes the terminal characteristics and the signals multiplexed on each pin. The following list describes the column headings in Table 2-1:

1. Ball: Ball number(s) associated with each signal(s)
2. Pin Name: Names of all the signals that are multiplexed on each ball
3. A/D: Analog or digital signal
4. Type: Terminal type when a particular signal is multiplexed on the terminal
   - I = Input
   - O = Output
   - OD = Open drain
5. Reference Level: Voltage applied to the I/O cell (see the power module and battery charger interface [BCI] chapters for values).
6. PU/PD: Denotes the presence of an internal pullup or pulldown. Pullups and pulldowns can be enabled or disabled through software.
7. Min = Minimum value
8. Typ = Typical value
9. Max = Maximum value
10. Buffer Strength: Drive strength of the associated output buffer

Table 2-1. Ball Characteristics

Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (kΩ)			PD[6] (kΩ)			Buffer Strength (mA)[10]
					Min[7]	Typ[8]	Max[9]	Min	Typ	Max	
H4	ADCIN0	A	I/O	VINTANA1.OUT							
J3	ADCIN1	A	I/O	VINTANA1.OUT							
G3	ADCIN2	A	I	VINTANA2.OUT							
P5	VCCS	A	I	VBAT + 0.2							
N5	VAC	A	Power	VACCHARGER							
P4	VBATS	A	I	VBAT							
N4	PCHGAC	A	I	VACCHARGER							
N6	PCHGUSB	A	I	VBUS							
N2	VPRECH	A	O	VPRECH							
N1	BCIAUTO	A	I	VPRECH							
P6	ICTLUSB1	A	O	VBUS							
P1	ICTLUSB2	A	O	VCCS							
N7	ICTLAC1	A	O	VACCHARGER							
P2	ICTLAC2	A	O	VCCS							
R5	VBAT	A	Power	VBAT							
P12	GPIO0/CD1	D	I/O	IO_1P8	75	100	202	59	100	144	8
	JTAG.TDO	D	I/O	IO_1P8							8
N12	GPIO1/CD2	D	I/O	IO_1P8	75	100	202	59	100	144	2
	JTAG.TMS	D	I	IO_1P8							
L4	GPIO2	D	I/O	IO_1P8	156	220	450	59	100	144	2
	Test1	D	I/O	IO_1P8							2
P13	GPIO15	D	I/O	IO_1P8	156	220	450	59	100	144	2
	Test2	D	I/O	IO_1P8							2
M4	GPIO6	D	I/O	IO_1P8	75	100	202	59	100	144	2
	PWM0	D	O	IO_1P8							4
	Test3	D	I/O	IO_1P8							2

Table 2-1. Ball Characteristics (continued)

Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (kΩ)			PD[6] (kΩ)			Buffer Strength (mA)[10]
					Min[7]	Typ[8]	Max[9]	Min	Typ	Max	
N14	GPIO7	D	I/O	IO_1P8	75	100	202	59	100	144	2
	VIBRA.SYNC	D	I	IO_1P8							
	PWM1	D	O	IO_1P8							4
	Test4	D	I/O	IO_1P8							2
J9	START.ADC	D	I	IO_1P8							
C13	SYSEN	D	OD/I	IO_1P8	4.7	7.35	10				2
C6	CLKEN	D	O	IO_1P8							2
D7	CLKEN2	D	O	IO_1P8							2
G10	CLKREQ	D	I	IO_1P8				60	100	146	
F10	INT1	D	O	IO_1P8							2
F9	INT2	D	O	IO_1P8							2
A13	NRESPWRON	D	O	IO_1P8							2
B13	NRESWARM	D	I	IO_1P8							2
A11	PWRON	D	I	VBAT							
B14	NC										
P7	NSLEEP1	D	I	IO_1P8							
G9	NSLEEP2	D	I	IO_1P8							
D13	CLK256FS(1)	D	O	IO_1P8							2
F8	VMODE1	D	I	IO_1P8							
K11	BOOT0	A/D	I/O	VBAT							
J11	BOOT1	A/D	I/O	VBAT							
A10	REGEN	D	OD	VBAT	5.5	8	12				2
H8	MSECURE	D	I	IO_1P8							
N16	VREF	A	Power	VREF							
N15	AGND	A	Power GND	GND							
C4	NC										
	I2C.SR.SDA	D	I/O	IO_1P8	2.5		3.4				12
D6	VMODE2	D	I	IO_1P8							2
	I2C.SR.SCL	D	I/O	IO_1P8	2.5		3.4				12
D4	I2C.CNTL.SDA	D	I/O	IO_1P8	2.5		3.4				12
D5	I2C.CNTL.SCL	D	I	IO_1P8	2.5		3.4				12
R1	PCM.VCK	D	I/O	IO_1P8							2
T2	PCM.VDR	D	I/O	IO_1P8							2
T15	PCM.VDX	D	I/O	IO_1P8							2
R16	PCM.VFS	D	I/O	IO_1P8							2
L3	I2S.CLK	D	I/O	IO_1P8							2
K6	I2S.SYNC	D	I/O	IO_1P8							2
K4	I2S.DIN	D	I	IO_1P8							2
K3	I2S.DOUT	D	O	IO_1P8							2
E2	MIC.MAIN.P	A	I	MICBIAS1.OUT							
F2	MIC.MAIN.M	A	I	MICBIAS1.OUT							
G2	MIC.SUB.P	A	I	MICBIAS2.OUT							
	DIG.MIC.0	A	I	VMIC1.OUT							
H2	MIC.SUB.M	A	I	MICBIAS2.OUT							
	DIG.MIC.1	A	I	VMIC2.OUT							
E3	HSMIC.P	A	I	VINTANA2.OUT							
F3	HSMIC.M	A	I	VINTANA2.OUT							
D10	VBAT.LEFT	A	Power	VBAT							
D9	VBAT.LEFT	A	Power	VBAT							
B9	IHF.LEFT.P	A	O	VBAT							
B10	IHF.LEFT.M	A	O	VBAT							
C10	GND.LEFT	A	Power GND	GND							
C9	GND.LEFT	A	Power GND	GND							
D12	VBAT.RIGHT	A	Power	VBAT							

(1) To avoid reflection on this pin caused by impedance mismatch, a serial resistance (Rs) of 33 Ω must be added.

Table 2-1. Ball Characteristics (continued)

Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (kΩ)			PD[6] (kΩ)			Buffer Strength (mA)[10]
					Min[7]	Typ[8]	Max[9]	Min	Typ	Max	
D11	VBAT.RIGHT	A	Power	VBAT							
B11	IHF.RIGHT.P	A	O	VBAT							
B12	IHF.RIGHT.M	A	O	VBAT							
C12	GND.RIGHT	A	Power GND	GND							
C11	GND.RIGHT	A	Power GND	GND							
A6	EAR.P	A	O	VINTANA2.OUT							
A7	EAR.M	A	O	VINTANA2.OUT							
B4	HSOL	A	O	VINTANA2.OUT							
B7	PreDriv.LEFT	A	O	VINTANA2.OUT							
	VMID	A	Power	VINTANA2.OUT							
B5	HSOR	A	O	VINTANA2.OUT							
B8	PreDriv.RIGHT	A	O	VINTANA2.OUT							
	ADCIN7	A	I	VINTANA2.OUT							
F1	AUXL	A	I	VINTANA2.OUT							
G1	AUXR	A	I	VINTANA2.OUT							
D1	MICBIAS1.OUT	A	Power	VINTANA2.OUT							
	VMIC1.OUT	A	Power	VINTANA2.OUT							
D2	MICBIAS2.OUT	A	Power	VINTANA2.OUT							
	VMIC2.OUT	A	Power	VINTANA2.OUT							
E4	VHSMIC.OUT	A	Power	VINTANA2.OUT							
D3	MICBIAS.GND		Power GND	GND							
J4 / J6 /J7 / J8 / E5	AVSS1	A	Power GND	GND							
R10	AVSS2	A	Power GND	GND							
M15	AVSS3	A	Power GND	GND							
C7	AVSS4	A	Power GND	GND							
B1	UART1.TXD	D	OD	External 1.8 to 3.3 V							2
D8	GPIO8	D	I	IO_1P8	4.7	7.4	10	5.9	7	8.3	
	UART1.RXD	D	I	IO_1P8							
N11	RTSO/ CLK64K.OUT/ BERCLK.OUT	D	OD	VUSB.3P1							2
	ADCIN5	A	I	VINTANA2.OUT							
P11	CTSI/ BERDATA.OUT	D	OD/CMOS/I/O	VUSB.3P1	4.7	7.4	10				2
	ADCIN3	A	I	VINTANA2.OUT							
N8	TXAF	A	I	VUSB.3P1							
	ADCIN4	A	I	VINTANA2.OUT							
N9	RXAF	A	O	VUSB.3P1							
	ADCIN6	A	I	VINTANA2.OUT							
L10	MANU	D	I	VUSB.3P1	162	280	414				
N10	32KCLKOUT	D	O	IO_1P8							
P16	32KXIN	A	I	IO_1P8							
P15	32KXOUT	A	O	IO_1P8							
A14	HFCLKIN	A	I	IO_1P8							
R12	HFCLKOUT	D	O	IO_1P8							
R8	VBUS	A	Power	VBUS							
T10	DP/UART3.RXD	A	I/O	VBUS							2
T11	DN/UART3.TXD	A	I/O	VBUS							2
R11	ID	A	I/O	VBUS							2
L15	UCLK	D	I	IO_1P8							16
L14	STP	D	I	IO_1P8	75	100	202	59	100	144	16
	GPIO9	D	I/O	IO_1P8							2
L13	DIR	D	O	IO_1P8	75	100	202	59	100	144	16
	GPIO10	D	I/O	IO_1P8							2

Table 2-1. Ball Characteristics (continued)

Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (kΩ) Min[7]	PU[6] (kΩ) Typ[8]	PU[6] (kΩ) Max[9]	PD[6] (kΩ) Min	PD[6] (kΩ) Typ	PD[6] (kΩ) Max	Buffer Strength (mA)[10]
M13	NXT	D	O	IO_1P8	75	100	202	59	100	144	16
	GPIO11	D	I/O	IO_1P8							2
K14	DATA0	D	I/O	IO_1P8							16
	UART4.TXD	D	I	IO_1P8							
K13	DATA1	D	I/O	IO_1P8							16
	UART4.RXD	D	O	IO_1P8							2
J14	DATA2	D	I/O	IO_1P8							16
	UART4.RTSI	D	I	IO_1P8							
J13	DATA3	D	I/O	IO_1P8	60	100	140	60	100	140	16
	UART4.CTSO	D	O	IO_1P8							16
	GPIO12	D	I/O	IO_1P8	75	100	202	59	100	144	16
G14	DATA4	D	I/O	IO_1P8	75	100	202	59	100	144	16
	GPIO14	D	I/O	IO_1P8							2
G13	DATA5	D	I/O	IO_1P8	75	100	202	59	100	144	16
	GPIO3	D	I/O	IO_1P8							2
F14	DATA6	D	I/O	IO_1P8	75	100	202	59	100	144	16
	GPIO4	D	I/O	IO_1P8							2
F13	DATA7	D	I/O	IO_1P8	75	100	202	59	100	144	16
	GPIO5	D	I/O	IO_1P8							2
T16	TEST.RESET	A/D	I	VBAT				30	50	70	
T1	TESTV1	A	I/O	VBAT							
A16	TESTV2	A	I/O	VINTANA2.OUT							
A1	TEST	D	I	IO_1P8				60	100	146	
A15	JTAG.TDI/ BERDATA	D	I	IO_1P8							
B16	JTAG.TCK/ BERCLK	D	I	IO_1P8							
R7	CP.IN	A	Power	VBAT/VBUS							
T7	CP.CAPP	A	O	CP.CAPP							
T6	CP.CAPM	A	O	CP.CAPM							
R6	CP.GND	A	Power GND	GND							
R9	VBAT.USB	A	Power	VBAT							
P9	VUSB.3P1	A	Power	VUSB.3P1							
L1	VAUX12S.IN	A	Power	VBAT							
M2	VAUX1.OUT	A	Power	VAUX1.OUT							
M3	VAUX2.OUT	A	Power	VAUX2.OUT							
H15	VPLLA3R.IN	A	Power	VBAT							
K16	VRTC.OUT	A	Power	VRTC.OUT							
H14	VPLL1.OUT	A	Power	VPLL1.OUT							
J15	VSDI.CSI.OUT	A	Power	VSDI.CSI.OUT							
G16	VAUX3.OUT	A	Power	VAUX3.OUT							
B2	VAUX4.IN	A	Power	VBAT							
B3	VAUX4.OUT	A	Power	VAUX4.OUT							
C1	VMMC1.IN	A	Power	VBAT							
C2	VMMC1.OUT	A	Power	VMMC1.OUT							
A3	VMMC2.IN	A	Power	VBAT							
A4	VMMC2.OUT	A	Power	VMMC2.OUT							
K2	VSIM.OUT	A	Power	VSIM.OUT							
P8	VINTUSB1P5. OUT	A	Power	VINTUSB1P5.OUT							
P10	VINTUSB1P8. OUT	A	Power	VINTUSB1P8.OUT							
K1	VDAC.IN	A	Power	VBAT							
L2	VDAC.OUT	A	Power	VDAC.OUT							
K15	VINT.IN	A	Power	VBAT							
H3	VINTANA1.OUT	A	Power	VINTANA1.OUT							

Table 2-1. Ball Characteristics (continued)

Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (kΩ)			PD[6] (kΩ)			Buffer Strength (mA)[10]
					Min[7]	Typ[8]	Max[9]	Min	Typ	Max	
J2	VINTANA2.OUT	A	Power	VINTANA2.OUT							
B6	VINTANA2.OUT	A	Power	VINTANA2.OUT							
L16	VINTDIG.OUT	A	Power	VINTDIG.OUT							
E15	VDD1.IN	A	Power	VBAT							
E14	VDD1.IN	A	Power	VBAT							
D14	VDD1.IN	A	Power	VBAT							
D16	VDD1.SW	A	O	VBAT							
D15	VDD1.SW	A	O	VBAT							
C14	VDD1.SW	A	O	VBAT							
E13	VDD1.FB	A	I								
C16	VDD1.GND	A	Power GND	GND							
C15	VDD1.GND	A	Power GND	GND							
B15	VDD1.GND	A	Power GND	GND							
R13	VDD2.IN	A	Power	VBAT							
P14	VDD2.IN	A	Power	VBAT							
N13	VDD2.FB	A	I								
T13	VDD2.SW	A	O	VBAT							
R14	VDD2.SW	A	O	VBAT							
T14	VDD2.GND	A	Power GND	GND							
R15	VDD2.GND	A	Power GND	GND							
P3	VIO.IN	A	Power	VBAT							
R4	VIO.IN	A	Power	VBAT							
N3	VIO.FB	A	I								
R3	VIO.SW	A	O	VBAT							
T4	VIO.SW	A	O	VBAT							
R2	VIO.GND	A	Power GND	GND							
T3	VIO.GND	A	Power GND	GND							
M14	BKBAT	A	Power	VBACK							
C8	IO.1P8	A	Power	IO_1P8							
H13 / H9 / H10 / H11	DGND	A	Power GND	GND							
F16	LEDGND	A	Power GND	GND							
G11	GPIO13	D	I/O	IO_1P8	75	100	202	59	100	144	
	LEDSYNC	D	I	IO_1P8							
F15	LEDA	A	OD	VBAT							
	VIBRA.P	A	OD	VBAT							
G15	LEDB	A	OD	VBAT							
	VIBRA.M	A	OD	VBAT							
G8	KPD.C0	D	OD	IO_1P8							
H7	KPD.C1	D	OD	IO_1P8							
G6	KPD.C2	D	OD	IO_1P8							
F7	KPD.C3	D	OD	IO_1P8							
G7	KPD.C4	D	OD	IO_1P8							
F4	KPD.C5	D	OD	IO_1P8							
H6	KPD.C6	D	OD	IO_1P8							
G4	KPD.C7	D	OD	IO_1P8							
K9	KPD.R0	D	I	IO_1P8	8	10	12				
K8	KPD.R1	D	I	IO_1P8	8	10	12				
L8	KPD.R2	D	I	IO_1P8	8	10	12				
K7	KPD.R3	D	I	IO_1P8	8	10	12				
L9	KPD.R4	D	I	IO_1P8	8	10	12				
J10	KPD.R5	D	I	IO_1P8	8	10	12				
K10	KPD.R6	D	I	IO_1P8	8	10	12				
L7	KPD.R7	D	I	IO_1P8	8	10	12				

Table 2-1. Ball Characteristics (continued)

Ball[1]	Pin Name[2]	A/D [3]	Type[4]	Reference Level RL[5]	PU[6] (kΩ)			PD[6] (kΩ)			Buffer Strength (mA)[10]
					Min[7]	Typ[8]	Max[9]	Min	Typ	Max	
C3	GPIO16	D	I/O	IO_1P8	75	100	202	59	100	144	
	BT.PCM.VDR	D	I/O	IO_1P8							
	DIG.MIC.CLK0	D	O	IO_1P8							
C5	GPIO17	D	I/O	IO_1P8	75	100	202	59	100	144	
	BT.PCM.VDX	D	I/O	IO_1P8							
	DIG.MIC.CLK1	D	O	IO_1P8							
A2	RFID.EN	D	O	VMMC2.OUT							

2.3 Signal Description

Table 2-2 lists the signals on the TPS65950; some signals are available on multiple pins.

Table 2-2. Signal Description

Module	Signal Name	Description	Type(1)	Ball	Configuration By Default After Reset Released			Unused Features(2)
					Signal	Type(1)	Internal Pull or Not	
ADC	ADCIN0	Battery type	I/O	H4	ADCIN0	I		GND
	ADCIN1	Battery temperature	I/O	J3	ADCIN1	I		GND
	ADCIN2	General-purpose (GP) ADC input	I	G3	ADCIN2	I		GND
Charger	VCCS	Charge current sensing	I	P5	VCCS	I		Cap to GND(3)
	VAC	Charge device input voltage	Power	N5	VAC	Power		GND
	VBATS	Charge current sensing	I	P4	VBATS	I		Cap to GND(3)
	PCHGAC	ac precharge sense signal. Used also for EEPROM	I	N4	PCHGAC	I		GND
	PCHGUSB	USB precharge sense signal	I	N6	PCHGUSB	I		GND
	VPRECH	Precharge regulator output	O	N2	VPRECH	O		Cap to GND(3)
	BCIAUTO	Linear charge specific boot mode	I	N1	BCIAUTO	I		GND
	ICTLUSB1	USB power device control	O	P6	ICTLUSB1	O		Floating
	ICTLUSB2	USB power device control	O	P1	ICTLUSB2	O		Floating
	ICTLAC1	ac power device control	O	N7	ICTLAC1	O		Floating
	ICTLAC2	ac power device control	O	P2	ICTLAC2	O		Floating
	VBAT	Battery voltage sensing	Power	R5	VBAT	Power		VBAT
GPIOs/ JTAG	GPIO0/CD1	GPIO0/card detection 1	I/O	P12	GPIO0	I	PD	Floating
	JTAG.TDO	JTAG test data output	I/O					
	GPIO1/CD2	GPIO1/card detection 2	I/O	N12	GPIO1	I	PD	Floating
	JTAG.TMS	JTAG test mode state	I					
	GPIO2	GPIO2	I/O	L4	GPIO2	I	PD	Floating
	Test1	Test1 pin used in test mode only	I/O					
	GPIO15	GPIO15	I/O	P13	GPIO15	I	PD	Floating
	Test2	Test2 pin used in test mode only	I/O					
	GPIO6	GPIO6	I/O	M4	GPIO6	I	PD	Floating
	PWM0	Pulse width driver 0	O					
	Test3	Test3 pin used in test mode only (controlled by JTAG)	I/O					
	GPIO7	GPIO7	I/O	N14	GPIO7	I	PD	Floating
	VIBRA.SYNC	Vibrator on-off synchronization	I					
	PWM1	Pulse width driver	O					
	Test4	Test4 pin used in test mode only (controlled by JTAG)	I/O					
START. ADC	START.ADC	ADC conversion request	I	J9	START.ADC	I		GND

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type[(1)]	Ball	Configuration By Default After Reset Released			Unused Features[(2)]
					Signal	Type[(1)]	Internal Pull or Not	
CONTROL	SYSEN	System enable output	OD/I	C13	SYSEN	OD	PU	Floating
	CLKEN	Clock enable	O	C6	CLKEN	O		Floating
	CLKEN2	Clock enable 2	O	D7	CLKEN2	O		Floating
	CLKREQ	Clock request	I	G10	CLKREQ	I	PD	GND
	INT1	Output interrupt line 1	O	F10	INT1	O		Floating
	INT2	Output interrupt line 2	O	F9	INT2	O		Floating
	NRESPWRON	Output control the NRESPWRON of the application processor	O	A13	NRESPWRON	O		Floating
	NRESWARM	Input, detect user action on the reset button	I	B13	NRESWARM	I		GND
	PWRON	Input, detect a control command to start or stop the system	I	A11	PWRON	I		VBAT
	NC	Not connected		B14	NC			Floating
	NSLEEP1	Sleep request from device 1	I	P7	NSLEEP1	I		GND
	NSLEEP2	Sleep request from device 2	I	G9	NSLEEP2	I		GND
	CLK256FS	Control for 256 × F_S CLK output	O	D13	CLK256FS	O		Floating
	VMODE1	Digital voltage scaling linked with VDD1	I	F8	VMODE1	I		GND
	BOOT0	Boot pin 0	I	K11	BOOT0	I	PD	N/A
	BOOT1	Boot pin 1	I	J11	BOOT1	I	PD	N/A
	REGEN	Enable signal for external LDO	OD	A10	REGEN	OD	PU	Floating
	MSECURE	Security and digital rights management	I	H8	MSECURE	I		N/A
VREF	VREF	Reference voltage	Power	N16	VREF	Power		N/A
	AGND	Analog ground for reference voltage	Power GND	N15	AGND	Power GND		GND
I2C SmartReflex	NC	Not connected		C4	Signal not functional[(4)]			Floating
	I2C.SR.SDA	SmartReflex I2C data	I/O					
	VMODE2	Digital voltage scaling linked with VDD2	I	D6	VMODE2	I		GND
	I2C.SR.SCL	SmartReflex I2C data	I/O					
I2C	I2C.CNTL.SDA	GP I2C data	I/O	D4	I2C.CNTL.SDA	I/O	PU	N/A
	I2C.CNTL.SCL	GP I2C clock	I/O	D5	I2C.CNTL.SCL	I/O	PU	N/A
PCM	PCM.VCK	Data clock (voice port)	I/O	R1	PCM.VCK	I/O		Floating
	PCM.VDR	Data receive (voice port)	I/O	T2	PCM.VDR	I/O		GND
	PCM.VDX	Data transmit (voice port)	I/O	T15	PCM.VDX	I/O		Floating
	PCM.VFS	Frame synchronization (voice port)	I/O	R16	PCM.VFS	I/O		Floating
TDM	I2S.CLK	Clock signal (audio port)	I/O	L3	I2S.CLK	I/O		Floating
	I2S.SYNC	Synchronization signal (audio port)	I/O	K6	I2S.SYNC	I/O		Floating
	I2S.DIN	Data receive (audio port)	I	K4	I2S.DIN	I		GND
	I2S.DOUT	Data transmit (audio port)	O	K3	I2S.DOUT	O		Floating
ANA.MIC	MIC.MAIN.P	Main microphone left input (P)	I	E2	MIC.MAIN.P	I		Cap to GND
	MIC.MAIN.M	Main microphone left input (M)	I	F2	MIC.MAIN.M	I		Cap to GND
	MIC.SUB.P	Main microphone right input (P)	I	G2	MIC.SUB.P	I		Cap to GND
	DIG.MIC.0	Digital microphone 0 input data	I					
	MIC.SUB.M	Main microphone right input (M)	I	H2	MIC.SUB.M	I		Cap to GND
	DIG.MIC.1	Digital microphone 1 input data	I					
Headset microphone	HSMIC.P	Headset microphone input (P)	I	E3	HSMIC.P	I		Cap to GND
	HSMIC.M	Headset microphone input (M)	I	F3	HSMIC.M	I		Cap to GND

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type(1)	Ball	Configuration By Default After Reset Released			Unused Features(2)
					Signal	Type(1)	Internal Pull or Not	
Hands-free	VBAT.LEFT	Battery voltage input	Power	D10	VBAT.LEFT	Power		VBAT
	VBAT.LEFT	Battery voltage input	Power	D9	VBAT.LEFT	Power		VBAT
	IHF.LEFT.P	Hands-free speaker output left (P)	O	B9	IHF.LEFT.P	O		Floating
	IHF.LEFT.M	Hands-free speaker output left (M)	O	B10	IHF.LEFT.M	O		Floating
	GND.LEFT	GND	Power GND	C10	GND.LEFT	Power GND		GND
	GND.LEFT	GND	Power GND	C9	GND.LEFT	Power GND		GND
	VBAT.RIGHT	Battery voltage input	Power	D12	VBAT.RIGHT	Power		VBAT
	VBAT.RIGHT	Battery voltage input	Power	D11	VBAT.RIGHT	Power		VBAT
	GND.RIGHT	GND	Power GND	C12	GND.RIGHT	Power GND		GND
	GND.RIGHT	GND	Power GND	C11	GND.RIGHT	Power GND		GND
	IHF.RIGHT.P	Hands-free speaker output right (P)	O	B11	IHF.RIGHT.P	O		Floating
	IHF.RIGHT.M	Hands-free speaker output right (M)	O	B12	IHF.RIGHT.M	O		Floating
Earpiece	EAR.P	Earpiece output differential output (P)	O	A6	EAR.P	O		Floating
	EAR.M	Earpiece output differential output (M)	O	A7	EAR.M	O		Floating
Headset	HSOL	Differential/single-ended headset left output	O	B4	HSOL	O		Floating
	PreDriv.LEFT	Predriver output left P for external class-D amplifier	O	B7	VMID	Power		Floating
	VMID	Pseudo-ground for headset output	Power					
	HSOR	Differential/single-ended headset right output (P)	O	B5	HSOR	O		Floating
	PreDriv.RIGHT	Predriver output right P for external class-D amplifier	O	B8	ADCIN7	I		GND
	ADCIN7	GP ADC input 7	I					
AUX input	AUXL	Auxiliary audio input left	I	F1	AUXL	I		Cap to GND
	AUXR	Auxiliary audio input right	I	G1	AUXR	I		Cap to GND
VMIC BIAS	MICBIAS1.OUT	Analog microphone bias 1	Power	D1	MICBIAS1.OUT	Power		Floating
	VMIC1.OUT	Digital microphone power supply 1	Power					
	MICBIAS2.OUT	Analog microphone bias 2	Power	D2	MICBIAS2.OUT	Power		Floating
	VMIC2.OUT	Digital microphone power supply 2	Power					
	VHSMIC.OUT	Headset microphone bias	Power	E4	VHSMIC.OUT	Power		Floating
	MICBIAS.GND	Dedicated ground for microphones	Power GND	D3	MICBIAS.GND	Power GND		GND
	AVSS1	Analog ground	Power GND	J4/J6/J7/J8/E5	AVSS1	Power GND		GND
	AVSS2			R10	AVSS2			
	AVSS3			M15	AVSS3			
	AVSS4			C7	AVSS4			
Headset UART	UART1.TXD	Headset UART transmit data	OD	B1	UART1.TXD	OD	PU	Floating
	GPIO8	GPIO8	I/O	D8	GPIO8	I	PD	Floating
	UART1.RXD	Headset universal asynchronous receiver/transmitter (UART) receive data/switch detection	I					

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type(1)	Ball	Configuration By Default After Reset Released			Unused Features(2)
					Signal	Type(1)	Internal Pull or Not	
MCPC	RTSO/ CLK64K.OUT/ BERCLK.OUT	Ready-to-send output/ 64-kHz output clock/ Bit error ratio (BER) clock out in test mode	OD	N11	RTSO/ CLK64K.OUT/ BERCLK.OUT	OD		Floating
	ADCIN5	GP ADC input 5	I					
	CTSI/ BERDATA.OUT	Clear-to-send input/ BERDATAOUT in test mode	OD/ CMOS/ I/O	P11	CTSI/ BERDATA.OUT	OD		GND
	ADCIN3	GP ADC input 3	I					
	TXAF		I	N8	TXAF	I		Cap to GND
	ADCIN4	GP ADC input 4	I					
	RXAF		O	N9	RXAF	O		Floating
	ADCIN6	GP ADC input 6	I					
	MANU	Manufacturer pin	I	L10	MANU	I	PU	Floating
Clock	32KCLKOUT	Buffered output of the 32-kHz digital clock	O	N10	32KCLKOUT	O		Floating
	32KXIN	Input of the 32-kHz oscillator	I	P16	32KXIN	I		N/A
	32KXOUT	Output of the 32-kHz oscillator	O	P15	32KXOUT	O		Floating
	HFCLKIN	Input of the digital (or sine) HS clock	I	A14	HFCLKIN	I		N/A
	HFCLKOUT	HS clock output	O	R12	HFCLKOUT	O		Floating
USB PHY	VBUS	VBUS power rail	Power	R8	VBUS	Power		N/A
	DP/ UART3.RXD	USB data P/USB carkit receive data/UART3 receive data	I/O	T10	DP/UART3.RXD	I/O		N/A
	DN/ UART3.TXD	USB data N/USB carkit transmit data/UART3 transmit data	I/O	T11	DN/UART3.TXD	I/O		N/A
	ID	USB ID	I/O	R11	ID	I/O		Connected to VRUSB3V1
ULPI	UCLK	HS USB clock	I	L15	UCLK	O		Floating
	STP	HS USB stop	I	L14	STP	I	PU	Floating
	GPIO9	GPIO9	I/O					
	DIR	HS USB direction	O	L13	DIR	O		Floating
	GPIO10	GPIO10	I/O					
	NXT	HS USB next	O	M13	NXT	O		Floating
	GPIO11	GPIO11	I/O					
	DATA0	HS USB Data0	I/O	K14	DATA0	O		Floating
	UART4.TXD	UART4.TXD	I					
	DATA1	HS USB Data1	I/O	K13	DATA1	O		Floating
	UART4.RXD	UART4.RXD	O					
	DATA2	HS USB Data2	I/O	J14	DATA2	O		Floating
	UART4.RTSI	UART4.RTSI	I					
	DATA3	HS USB Data3	I/O	J13	DATA3	O		Floating
	UART4.CTSO	UART4.CTSO	O					
	GPIO12	GPIO12	I/O					
	DATA4	HS USB Data4	I/O	G14	DATA4	O		Floating
	GPIO14	GPIO14	I/O					
	DATA5	HS USB Data5	I/O	G13	DATA5	O		Floating
	GPIO3	GPIO3	I/O					
	DATA6	HS USB Data6	I/O	F14	DATA6	O		Floating
	GPIO4	GPIO4	I/O					
	DATA7	HS USB Data7	I/O	F13	DATA7	O		Floating
	GPIO5	GPIO5	I/O					

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type(1)	Ball	Configuration By Default After Reset Released			Unused Features(2)
					Signal	Type(1)	Internal Pull or Not	
Test	Test.RESET	Reset T2 device (except power state-machine)	I	T16	Test.RESET	I	PD	GND
	TestV1	Analog test	I/O	T1	TestV1	I/O		Floating
	TestV2	Analog test	I/O	A16	TestV2	I/O		Floating
	Test	Selection between JTAG mode and application mode for JTAG/GPIOs (with PU or PD)	I	A1	Test	I	PD	Floating
	JTAG.TDI/ BERDATA	JTAG.TDI/BERDATA	I	A15	JTAG.TDI/ BERDATA	I		GND
	JTAG.TCK/ BERCLK	JTAG.TCK/BERCLK	I	B16	JTAG.TCK/ BERCLK	I		GND
USB CP	CP.IN	CP input voltage	Power	R7	CP.IN	Power		VBAT
	CP.CAPP	CP flying capacitor P	O	T7	CP.CAPP	O		Floating
	CP.CAPM	CP flying capacitor M	O	T6	CP.CAPM	O		Floating
	CP.GND	CP ground	Power GND	R6	CP.GND	Power GND		GND
VBAT.USB	VBAT.USB	USB LDOs (VINTUSB1P5, VINTUSB1P8, VUSB.3P1) VBAT	Power	R9	VBAT.USB	Power		VBAT
USB.LDO	VUSB.3P1	USB LDO output	Power	P9	VUSB.3P1	Power		N/A
VAUX1	VAUX12S.IN	VAUX1/VAUX2/VSIM LDO input voltage	Power	L1	VAUX12S.IN	Power		VBAT
	VAUX1.OUT	VAUX1 LDO output voltage	Power	M2	VAUX1.OUT	Power		Floating
VAUX2	VAUX2.OUT	VAUX2 LDO output voltage	Power	M3	VAUX2.OUT	Power		Floating
VPLLA3R	VPLLA3R.IN	Input for VPLL1, VPLL2, VAUX3, VRTC LDOs	Power	H15	VPLLA3R.IN	Power		VBAT
VRTC	VRTC.OUT	VRTC internal LDO output (internal use only)	Power	K16	VRTC.OUT	Power		N/A
VPLL1	VPLL1.OUT	LDO output voltage	Power	H14	VPLL1.OUT	Power		Floating
VPLL2	VSDI.CSI.OUT	Output voltage of the regulator	Power	J15	VSDI.CSI.OUT	Power		Floating
VAUX3	VAUX3.OUT	VAUX3 LDO output voltage	Power	G16	VAUX3.OUT	Power		Floating
VAUX4	VAUX4.IN	VAUX4 LDO input voltage	Power	B2	VAUX4.IN	Power		VBAT
	VAUX4.OUT	VAUX4 LDO output voltage	Power	B3	VAUX4.OUT	Power		Floating
VMMC1	VMMC1.IN	VMMC1 LDO input voltage	Power	C1	VMMC1.IN	Power		VBAT
	VMMC1.OUT	VMMC1 LDO output voltage	Power	C2	VMMC1.OUT	Power		Floating
VMMC2	VMMC2.IN	VMMC2 LDO input voltage	Power	A3	VMMC2.IN	Power		VBAT
	VMMC2.OUT	VMMC2 LDO output voltage	Power	A4	VMMC2.OUT	Power		Floating
VSIM	VSIM.OUT	VSIM LDO output voltage	Power	K2	VSIM.OUT	Power		Floating
VINTUSB1 P5	VINTUSB1P5. OUT	VINTUSB1P5 internal LDO output (internal use only)	Power	P8	VINTUSB1P5. OUT	Power		Floating
VINTUSB1 P8	VINTUSB1P8. OUT	VINTUSB1P8 internal LDO output (internal use only)	Power	P10	VINTUSB1P8. OUT	Power		Floating
Video DAC	VDAC.IN	Input for VDAC, VINTANA1, and VINTANA2 LDOs	Power	K1	VDAC.IN	Power		VBAT
	VDAC.OUT	Output voltage of the regulator	Power	L2	VDAC.OUT	Power		Floating
VINT	VINT.IN	Input for VINTDIG LDO	Power	K15	VINT.IN	Power		VBAT
VINTANA1	VINTANA1. OUT	VINTANA1 internal LDO output (internal use only)	Power	H3	VINTANA1.OUT	Power		N/A
VINTANA2	VINTANA2. OUT	VINTANA2 internal LDO output (internal use only)	Power	J2	VINTANA2.OUT	Power		N/A
	VINTANA2. OUT	VINTANA2 internal LDO output (internal use only)	Power	B6	VINTANA2.OUT	Power		N/A
VINTDIG	VINTDIG.OUT	VINTDIG internal LDO output (internal use only)	Power	L16	VINTDIG.OUT	Power		N/A

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type(1)	Ball	Configuration By Default After Reset Released			Unused Features(2)
					Signal	Type(1)	Internal Pull or Not	
VDD1	VDD1.IN	VDD1 dc-dc input voltage	Power	E15	VDD1.IN	Power		VBAT
	VDD1.IN	VDD1 dc-dc input voltage	Power	E14	VDD1.IN	Power		VBAT
	VDD1.IN	VDD1 dc-dc input voltage	Power	D14	VDD1.IN	Power		VBAT
	VDD1.SW	VDD1 dc-dc switch	O	D16	VDD1.SW	O		Floating
	VDD1.SW	VDD1 dc-dc switch	O	D15	VDD1.SW	O		Floating
	VDD1.SW	VDD1 dc-dc switch	O	C14	VDD1.SW	O		Floating
	VDD1.FB	VDD1 dc-dc output voltage (feedback)	I	E13	VDD1.FB	I		GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	C16	VDD1.GND	Power GND		GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	C15	VDD1.GND	Power GND		GND
	VDD1.GND	VDD1 dc-dc ground	Power GND	B15	VDD1.GND	Power GND		GND
VDD2	VDD2.IN	VDD2 dc-dc input voltage	Power	R13	VDD2.IN	Power		VBAT
	VDD2.IN	VDD2 dc-dc input voltage	Power	P14	VDD2.IN	Power		VBAT
	VDD2.FB	VDD2 dc-dc output voltage (feedback)	I	N13	VDD2.FB	I		GND
	VDD2.SW	VDD2 dc-dc switch	O	T13	VDD2.SW	O		Floating
	VDD2.SW	VDD2 dc-dc switch	O	R14	VDD2.SW	O		Floating
	VDD2.GND	VDD2 dc-dc ground	Power GND	T14	VDD2.GND	Power GND		GND
	VDD2.GND	VDD2 dc-dc ground	Power GND	R15	VDD2.GND	Power GND		GND
VIO	VIO.IN	VIO dc-dc input voltage	Power	P3	VIO.IN	Power		VBAT
	VIO.IN	VIO dc-dc input voltage	Power	R4	VIO.IN	Power		VBAT
	VIO.FB	VIO dc-dc output voltage (feedback)	I	N3	VIO.FB	I		GND
	VIO.SW	VIO dc-dc switch	O	R3	VIO.SW	O		Floating
	VIO.SW	VIO dc-dc switch	O	T4	VIO.SW	O		Floating
	VIO.GND	VIO dc-dc ground	Power GND	R2	VIO.GND	Power GND		GND
	VIO.GND	VIO dc-dc ground	Power GND	T3	VIO.GND	Power GND		GND
Backup battery	BKBAT	Backup battery	Power	M14	BKBAT	Power		GND
Digital VDD	IO.1P8	TPS65950 I/O input	Power	C8	IO.1P8	Power		N/A
Digital ground	DGND	Digital ground	Power GND	H13 / H9 / H10 / H11	DGND	Power GND		GND
LED driver	LEDGND	LED driver ground	Power GND	F16	LEDGND	Power GND		GND
	GPIO13	GPIO13	I/O	G11	GPIO13	I	PD	Floating
	LEDSYNC	LED synchronization input	I					
	LEDA	LED leg A	OD	F15	Signal not functional(4)			Floating
	VIBRA.P	H-bridge vibrator P						
	LEDB	LED leg B	OD	G15	Signal not functional(4)			Floating
	VIBRA.M	H-bridge vibrator M						

Table 2-2. Signal Description (continued)

Module	Signal Name	Description	Type(1)	Ball	Configuration By Default After Reset Released			Unused Features(2)
					Signal	Type(1)	Internal Pull or Not	
Keypad	KPD.C0	Keypad column 0	OD	G8	KPD.C0	OD		Floating
	KPD.C1	Keypad column 1	OD	H7	KPD.C1	OD		Floating
	KPD.C2	Keypad column 2	OD	G6	KPD.C2	OD		Floating
	KPD.C3	Keypad column 3	OD	F7	KPD.C3	OD		Floating
	KPD.C4	Keypad column 4	OD	G7	KPD.C4	OD		Floating
	KPD.C5	Keypad column 5	OD	F4	KPD.C5	OD		Floating
	KPD.C6	Keypad column 6	OD	H6	KPD.C6	OD		Floating
	KPD.C7	Keypad column 7	OD	G4	KPD.C7	OD		Floating
	KPD.R0	Keypad row 0	I	K9	KPD.R0	I	PU	Floating
	KPD.R1	Keypad row 1	I	K8	KPD.R1	I	PU	Floating
	KPD.R2	Keypad row 2	I	L8	KPD.R2	I	PU	Floating
	KPD.R3	Keypad row 3	I	K7	KPD.R3	I	PU	Floating
	KPD.R4	Keypad row 4	I	L9	KPD.R4	I	PU	Floating
	KPD.R5	Keypad row 5	I	J10	KPD.R5	I	PU	Floating
	KPD.R6	Keypad row 6	I	K10	KPD.R6	I	PU	Floating
	KPD.R7	Keypad row 7	I	L7	KPD.R7	I	PU	Floating
Bluetooth/ digital microphone	GPIO16	Bluetooth PCM receive data	I/O	C3	GPIO16	I	PD	Floating
	BT.PCM.VDR	GPIO16	I/O					
	DIG.MIC.CLK0	Digital microphone clock 0	O					
	GPIO17	GPIO17	I/O	C5	GPIO17	I	PD	Floating
	BT.PCM.VDX	Bluetooth PCM transmit data						
	DIG.MIC.CLK1	Digital microphone clock 1	O					
RFID	RFID.EN	Enable for the radio frequency identification (RFID) device	O	A2	RFID.EN	O		Floating

(1) I = Input; O = Output; OD = Open drain

(2) This column provides the connection when the associated feature is not used or not connected. When there is a pin muxing, not all functions on the muxed pin are used. But even if a function is not used, the Default Configuration column applies.

Connection criteria:
- Analog pins:
  - For input: GND
  - For output: Floating (except VPRECH is connected to GND)
  - For I/O if input by default: GND (except for audio features input: capacitor to ground with a 100-nF typical value capacitor)
- Digital pins:
  - For input: GND (except keypad and STP are left floating)
  - For input and pullup: Floating
  - For output: Floating
  - For I/O and pullup: Floating

N/A (not applicable): When the associated feature is mandatory for good functioning of the TPS65950.

(3) The VPRECH, VBATS, and VCCS signals must be connected to each other and with the CPRECH capacitor to GND (see Section 8.2.3, *Configuration with BCI Not Used*).

(4) Signal not functional indicates that no signal is presented on the pad after a release reset.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3-1 lists the absolute maximum ratings.

Table 3-1. Absolute Maximum Ratings

Parameter	Test Conditions	Min	Typ	Max	Unit
Main battery supply voltage(1)		2.1		4.5	V
Voltage on any input	Where supply represents the voltage applied to the power supply pin associated with the input	0.0		1.0*Supply	V
Storage temperature range		–55		125	°C
Ambient temperature range		–40		85	°C
Junction temperature (T_J)	At 1.4W (Theta JB 11°C/W 2S2P board)			105	°C
Junction temperature (T_J) for parametric compliance		–40		105	°C

(1) The product can tolerate voltage spikes of 5.2 V for a total duration of 10 milliseconds.

3.2 Minimum Voltages and Associated Currents

Table 3-2 lists the VBAT minimum and maximum currents per VBAT ball.

Table 3-2. VBAT Min Required Per VBAT Ball and Associated Maximum Current

Category	Pin and Module	Maximum Current Specified (mA)	Output Voltage (V)	VBAT Minimum (V)
VBAT pin name	VDD_VPLLA3R_IN_6POV	340		
Internal module supplied	VPLL1 (LDO)	40	1.0 / 1.2 / 1.3 / 1.8 / 2.8 / 3.0	Maximum (2.7, output voltage selected + 250 mV)
	VPLL2 (LDO)	100	0.7 / 1.0 / 1.2 / 1.3 / 1.5 / 1.8 / 1.85 / 2.5 / 2.6 / 2.8 / 2.85 / 3.0 / 3.15	Maximum (2.7, output voltage selected + 250 mV)
	VAUX3 (LDO)	200	1.5 / 1.8 / 2.5 / 2.8 / 3.0	Maximum (2.7, output voltage selected + 250 mV)
	VDD1 core (DCDC)	< 1		2.7
	VDD2 core (DCDC)	< 1		2.7
	SYSPOR (power ref)	< 1		2.7
	PBIAS (power ref)	< 1		2.7
VBAT pin name	VDD_VDAC_IN_6POV	370		
Internal module supplied	VDAC (LDO)	70	1.2 / 1.3 / 1.8	Maximum (2.7, output voltage selected + 250 mV)
	VINTANA1 (LDO)	50	1.5	Maximum (2.7, output voltage selected + 250 mV)
	VINTANA2 (LDO)	250	2.5 / 2.75	Maximum (2.7, output voltage selected +250 mV)
	VIO core (DCDC)	< 1		2.7
	VAUX4 core (LDO)	< 1		2.7
VBAT pin name	VDD_VAUXI2S_IN_6POV	350		

Table 3-2. VBAT Min Required Per VBAT Ball and Associated Maximum Current (continued)

Category	Pin and Module	Maximum Current Specified (mA)	Output Voltage (V)	VBAT Minimum (V)
Internal module supplied	VAUX1 (LDO)	200	1.5 / 1.8 / 2.5 / 2.8 / 3.0	Maximum (2.7, output voltage selected + 250 mV)
	VAUX2 (LDO)	100	1.3 / 1.5 / 1.6 / 1.7 / 1.8 / 1.9 / 2.0 / 2.1 / 2.2 / 2.3 / 2.4 / 2.5 / 2.8	Maximum (2.7, output voltage selected + 250 mV)
	VSIM (LDO)	50	1.0 / 1.2 / 1.3 / 1.8 / 2.8 / 3.0	Maximum (2.7, output voltage selected + 250 mV)
VBAT pin name	VDD_VMMC2_IN_6POV	100		
	VMMC2 (LDO)	100	1.0 / 1.2 / 1.3 / 1.5 / 1.8 / 1.85 / 2.5 / 2.6 / 2.8 / 2.85 / 3.0 / 3.15	Maximum (2.7, output voltage selected + 250 mV)
	Power_REGBATT	0.001		2.7
VBAT pin name	VDD_VMMC1_IN_6POV	220		
	VMMC1 (LDO)	220	1.85 / 2.85 / 3.0 / 3.15	Maximum (2.7, output voltage selected + 250 mV)
	Power_REGBATT	0.001		2.7
VBAT pin name	VDD_VINT_IN_6POV	131		
Internal module supplied	VINTDIG (LDO)	80	1.0 / 1.2 / 1.3 / 1.5	Maximum (2.7, output voltage selected + 250 mV)
	VRRTC (LDO)	30	1.5	Maximum (2.7, output voltage selected + 250 mV)
	VBACKUP (LDO)	1	2.5 / 3.0 / 3.1 / 3.2	Maximum (2.7, output voltage selected + 250 mV)
VBAT pin name	VDD_VAUX4_IN_6POV	100		
	VAUX4 (LDO)	100	0.7 / 1.0 / 1.2 / 1.3 / 1.5 / 1.8 / 1.85 / 2.5 / 2.6 / 2.8 / 2.85 / 3.0 / 3.15	output voltage selected + 250 mV

3.3 Recommended Operating Conditions

Table 3-3 lists the recommended operating maximum ratings.

Table 3-3. Recommended Operating Maximum Ratings

Parameter	Min	Typ	Max	Unit
Main battery supply voltage	2.7[(1)]	3.6	4.5	V
Backup battery supply voltage	1.8	3.2	3.3	V
Ambient temperature range	–40		85	°C

(1) 2.7 V is the minimum threshold for the battery at which the device will turn OFF. However, the minimum voltage at which the device will power ON is 3.2 V ±100 mV (if PWRON does not have a switch and is connected to VBAT) considering battery plug as the device switch on event. If PWRON has a switch then 3.2 V is the minimum for the device to turn ON.

3.4 Digital I/O Electrical Characteristics

Table 3-4 describes the digital I/O electrical characteristics.

- RL: Reference level voltage applied to the I/O cell
- VOL: Low-level output voltage
- VOH: High-level output voltage
- VIL: Low-level input voltage
- VIH: High-level input voltage

Table 3-4. Digital I/O Electrical Characteristics

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIH (V)		Max Freq (MHz)	Load (pF) Output Mode	Rise Time (ns)	Fall Time (ns)
	Min	Max	Min	Max	Min	Max	Min	Max				
GPIO0/CD1 JTAG.TDO	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	33	30	5.2	5.2
GPIO0/CD2 JTAG.TMS	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	33	30	5.2	5.2
GPIO2 Test1	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
GPIO15 Test2	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
GPIO16 PWM0 Test3	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
GPIO17 VIBRA.SYNC PWM1 Test4	0	0.45	RL–0.45	RL	0	0.35xRL	0.65xRL	RL	3	30	5.2	5.2
START.ADC	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	6		16.7	16.7
SYSEN	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL			5.2	5.2
CLKEN	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
CLKEN2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
CLKREQ	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
INT1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
INT2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
NRESPWRON	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
NRESWARM	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
PWRON					0	0.35×1.8V	0.65×1.8V	VBAT	3		33.3	33.3
NSLEEP1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
NSLEEP2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
CLK256FS	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	12.288	30	16.3	16.3
VMODE1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
BOOT0	0							RL	3		33.3	33.3
BOOT1	0							RL	3		33.3	33.3
REGEN	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
MSECURE	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.3	33.3
I2C.SR.SDA	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4	Up to 400		
VMODE2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3.4		29.4	29.4
I2C.SR.SCL	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4		10.0	10.0
I2C.CNTL.SDA	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4	Up to 400		
I2C.CNTL.SCL	0	0.4			–0.5	0.3×RL	0.7×RL	RL+0.5	3.4		10.0	10.0
PCM.VCK	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	1	30	100.0	33.0
PCM.VDR	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	1	30	100.0	100.0
PCM.VDX	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	1	30	100.0	33.0
PCM.VFS	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	1	30	33.0	33.0
I2S.CLK	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	6.5	30	33.0	33.0
I2S.SYNC	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	6.5	30	33.0	33.0
I2S.DIN	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3.25	30	33.0	33.0
I2S.DOUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3.25	30	29.0	29.0
UART1.TXD	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.0	33.0
GPIO8 UART1.RXD	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
RTSO/CLD64K.OUT/ BERCLK.OUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.0	33.0
CTSI/BERDATA.OUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.0	33.0
MANU	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
32KCLKOUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.032	30	16	16
HFCLKOUT	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	38.4	30	2.6	2.6

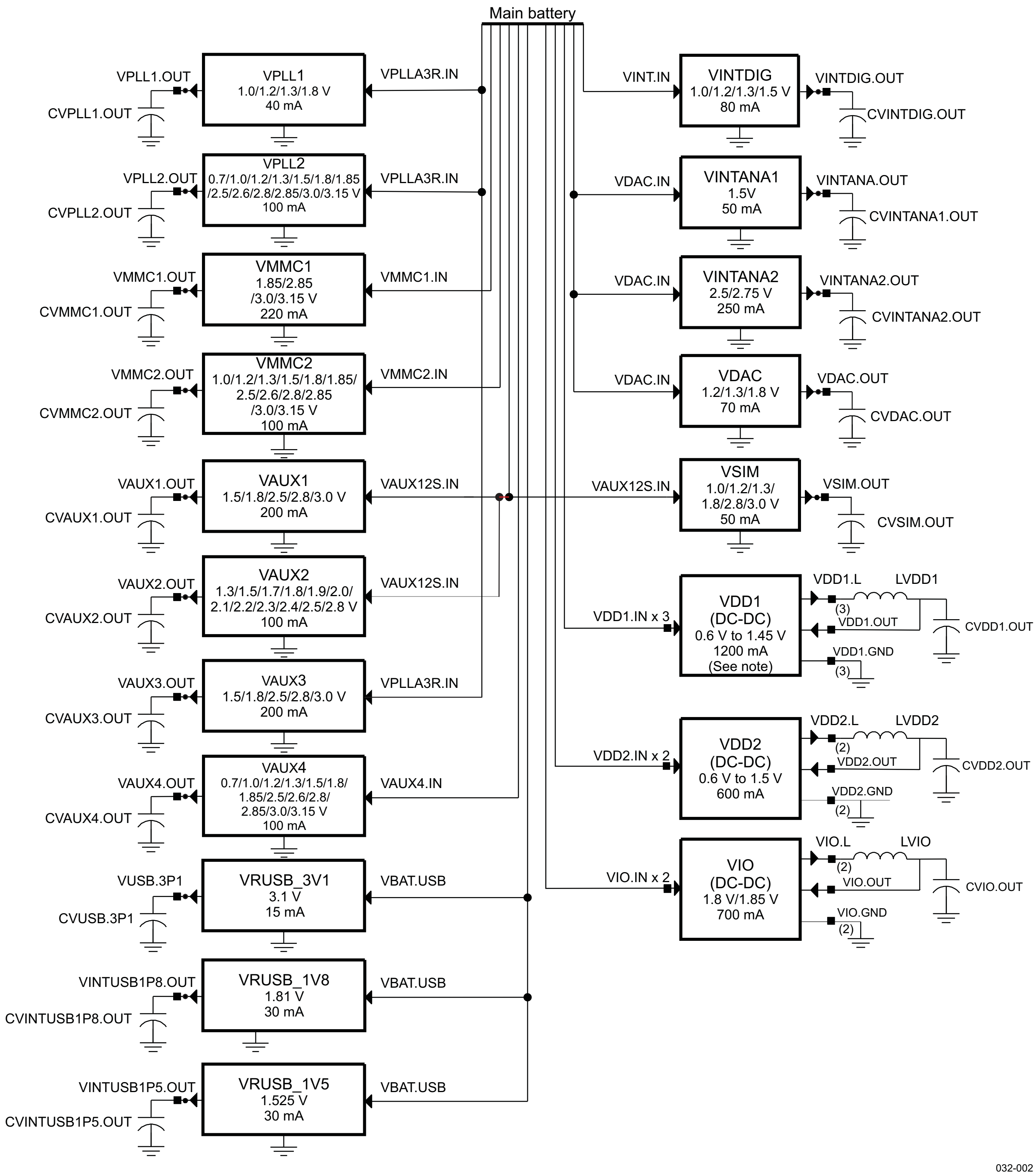
Table 3-4. Digital I/O Electrical Characteristics (continued)

Pin Name	VOL (V)		VOH (V)		VIL (V)		VIH (V)		Max Freq (MHz)	Load (pF) Output Mode	Rise Time (ns)	Fall Time (ns)
	Min	Max	Min	Max	Min	Max	Min	Max				
UCLK	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	60	10	1.0	1.0
STP GPIO9	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DIR GPIO10	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
NXT GPIO11	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA0 UART4.TXD	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA1 UART4.RXD	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA2 UART4.RTSI	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA3 UART4.CTSO	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
GPIO12	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA4 GPIO14	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA5 GPIO3	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA6 GPIO4	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
DATA7 GPIO5	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	30	10	1.0	1.0
Test.RESET	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
Test	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	29.0	29.0
JTAG.TDI/ BERDATA	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
JTAG.TCK/ BERDATA	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3		33.0	33.0
GPIO13 LEDSYNC	0	0.45	RL–0.45	RL	0	0.35×RL	0.35×RL		3	30	33.3	33.3
KPD.C0	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C3	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C4	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C5	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C6	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.C7	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033	30	29.0	29.0
KPD.R0	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R2	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R3	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R4	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R5	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R6	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
KPD.R7	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	0.033		3051.8	3051.8
GPIO16	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
DIG.MIC.CLK0	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	2.4	30	41.7	41.7
BT.PCM.VDX	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	1	30	100.0	100.0
GPIO17	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	3	30	33.3	33.3
DIG.MIC.CLK1	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	2.4	30	41.7	41.7
BT.PCM.VDX	0	0.45	RL–0.45	RL	0	0.35×RL	0.65×RL	RL	1	30	100.0	100.0
RFID.EN												

4 Power Module

This section describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled in the TPS65950.

Figure 4-1 is a block diagram of the power provider.



NOTE: For TPS65950A3: 0.6V to 1.2V, 1200mA and 1.2V to 1.45V, 1400mA

Figure 4-1. Power Provider Block Diagram

NOTE

For the component values, see Table 15-1.

4.1 Power Providers

Table 4-1 lists the power providers.

Table 4-1. Summary of the Power Providers

Name	Use	Type	Voltage Range (V)	Default Voltage Depending on Boot Mode[1]				Maximum Current
				OMAP2 Mode		OMAP3 Mode		
VAUX1	External	LDO	1.5, 1.8, 2.5, 2.8, 3.0	3.0 V		3.0 V		200 mA
VAUX2	External	LDO	1.3, 1.5, 1.7, 1.8, 1.9, 2.0, 2.1, 2.2, 2.3, 2.4, 2.5, 2.8	2.8 V		1.8 V		100 mA
VAUX3	External	LDO	1.5, 1.8, 2.5, 2.8, 3.0	2.8 V		2.8 V		200 mA
VAUX4	External	LDO	0.7, 1.0, 1.2, 1.3 1.5, 1.8, 1.85, 2.5, 2.6, 2.8, 2.85, 3.0, 3.15	1.2 V		2.8 V		100 mA
VMMC1	External	LDO	1.85, 2.85, 3.0, 3.15	1.85 V		3.0 V		220 mA
VMMC2	External	LDO	1.0, 1.2, 1.3, 1.5, 1.8, 1.85, 2.5, 2.6, 2.8, 2.85, 3.0, 3.15	2.6 V		2.6 V		100 mA
VPLL1	External	LDO	1.0, 1.2, 1.3, 1.8, 2.8, 3.0	1.3 V		1.8 V		40 mA
VPLL2	External	LDO	0.7, 1.0, 1.2, 1.3, 1.5, 1.8, 1.85, 2.5, 2.6, 2.8, 2.85, 3.0, 3.15	1.3 V		1.3 V		100 mA
VSIM	External	LDO	1.0, 1.2, 1.3, 1.8, 2.8, 3.0	1.8 V		1.8 V		50 mA
VDAC	External	LDO	1.2, 1.3, 1.8	1.8 V		1.8 V		70 mA
VIO	External	SMPS	1.8, 1.85	1.8 V		1.8 V		700 mA
VDD1 for TPS65950A2/ TPS65950A3	External	SMPS	0.6 ... 1.45	1.3 V		1.2 V		1200 mA
VDD1 for TPS65950A3	External	SMPS	1.2 ... 1.45	1.3 V		1.2 V		1400mA
VDD2	External	SMPS	0.6 ... 1.5	1.3 V		1.2 V		600 mA
VINTANA1	Internal	LDO	1.5	1.5 V		1.5 V		50 mA
VINTANA2	Internal	LDO	2.5, 2.75	2.75 V		2.75 V		250 mA
VINTDIG	Internal	LDO	1.0, 1.2, 1.3, 1.5	1.5 V		1.5 V		80 mA
USBCP	Internal	CP	5	5 V		5 V		100 mA
VUSB1V5	Internal	LDO	1.5	1.5 V		1.5 V		30 mA
VUSB1V8	Internal	LDO	1.8	1.8 V		1.8 V		30 mA
VUSB3V1	Internal	LDO	3.1	3.1 V		3.1 V		15 mA
VRRTC	Internal	LDO	1.5	1.5 V		1.5 V		30 mA
VBRTC	Internal	LDO	1.3	1.3 V		1.3 V		100 μA

(1) For the significance of boot mode, see Section 4.5, *Power Management.*

4.1.1 VDD1 dc-dc Regulator

4.1.1.1 VDD1 dc-dc Regulator Characteristics

The VDD1 dc-dc regulator is a stepdown dc-dc converter with a configurable output voltage. The programming of the output voltage and the characteristics of the dc-dc converter are SmartReflex-compatible. The regulator can be put in sleep mode to reduce its leakage (PFM) or power-down mode when it is not being used. Table 4-3 lists the characteristics of the regulator.

Table 4-2. Part Names With Corresponding VDD1 Current Support

Device Name	VDD1 Current Support
TPS65950A2ZXN/R (some bug fixes, see errata)	1.2 A
TPS65950A3ZXN/R (same as TPS65950A2 + 1 GHz support with higher current support)	1.4 A

Table 4-3. VDD1 dc-dc Regulator Characteristics

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6		1.45	V
Output voltage step	Covering the 0.6 to 1.45-V range		12.5		mV
Output accuracy (1)	0.6 to < 0.8 V	–6%		6%	
	0.8 to 1.45 V	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency (2), Figure 4-2 in active and sleep modes	I_O = 10 mA, sleep		82%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
	600 mA < I_O < 800 mA		75%		
Output current	Active mode, Output Voltage 0.6 V to 1.45 V for TPS65950A2/TPS65950A3			1200	mA
	Active mode, Output Voltage 1.2 V to1.45 V for TPS65950A3			1400	mA
	Sleep mode			10	mA
Ground current (I_Q)	Off at 30°C			3	μA
	Sleep, unloaded		30	50	
	Active, unloaded, not switching			300	
Short-circuit current	$V_{IN} = V_{Max}$		2.2		A
Load regulation	$0 < I_O < I_{Max}$			20	mV
Transient load regulation (3)	I_O = 10 mA to 600 +10 mA, Maximum slew rate is 600mA/100 ns.	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV_{PP} ac input, 10-μs rise and fall time			10	mV
Startup time			0.25	1	ms
Recovery time	From sleep mode to on mode with constant load		<10	100	μs
Slew rate (rising or falling) (4)		4	8	16	mV/μs
Output shunt resistor (pulldown)			500	700	Ω

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process). Under current load condition step: 600 mA in 100 ns with a ±20% external capacitor accuracy or 400 mA in 100 ns with a ±50% external capacitor accuracy
(2) VBAT = 3.6 V, VDD1 = 1.2 V, Fs = 3.2 MHz, L = 1 μH, L_{DCR} = 100 mΩ, C = 10 μF, ESR = 10 mΩ
(3) For negative transient load, the output voltage must discharge completely and settle to its final value within 100 ms. Transient load is specified at Vout max with a ±50% external capacitor accuracy and includes temperature and process variation.
(4) Load current varies proportionally with the output voltage. The slew rate is for increasing and decreasing voltages and the maximum load current is 1.1 A.

Table 4-3. VDD1 dc-dc Regulator Characteristics (continued)

Parameter	Comments	Min	Typ	Max	Unit
External coil	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current for TPS65950A2	1.8			A
	Saturation current for TPS65950A3	2.1			
External capacitor[1]	Value	8	10	12	µF
	Equivalent series resistance (ESR) at switching frequency	0		20	mΩ

See Table 2-2 for how to connect the VDD1/2 dc-dc converter when it is not used.

Figure 4-2 shows the efficiency of the VDD1 dc-dc regulator in active and sleep modes.

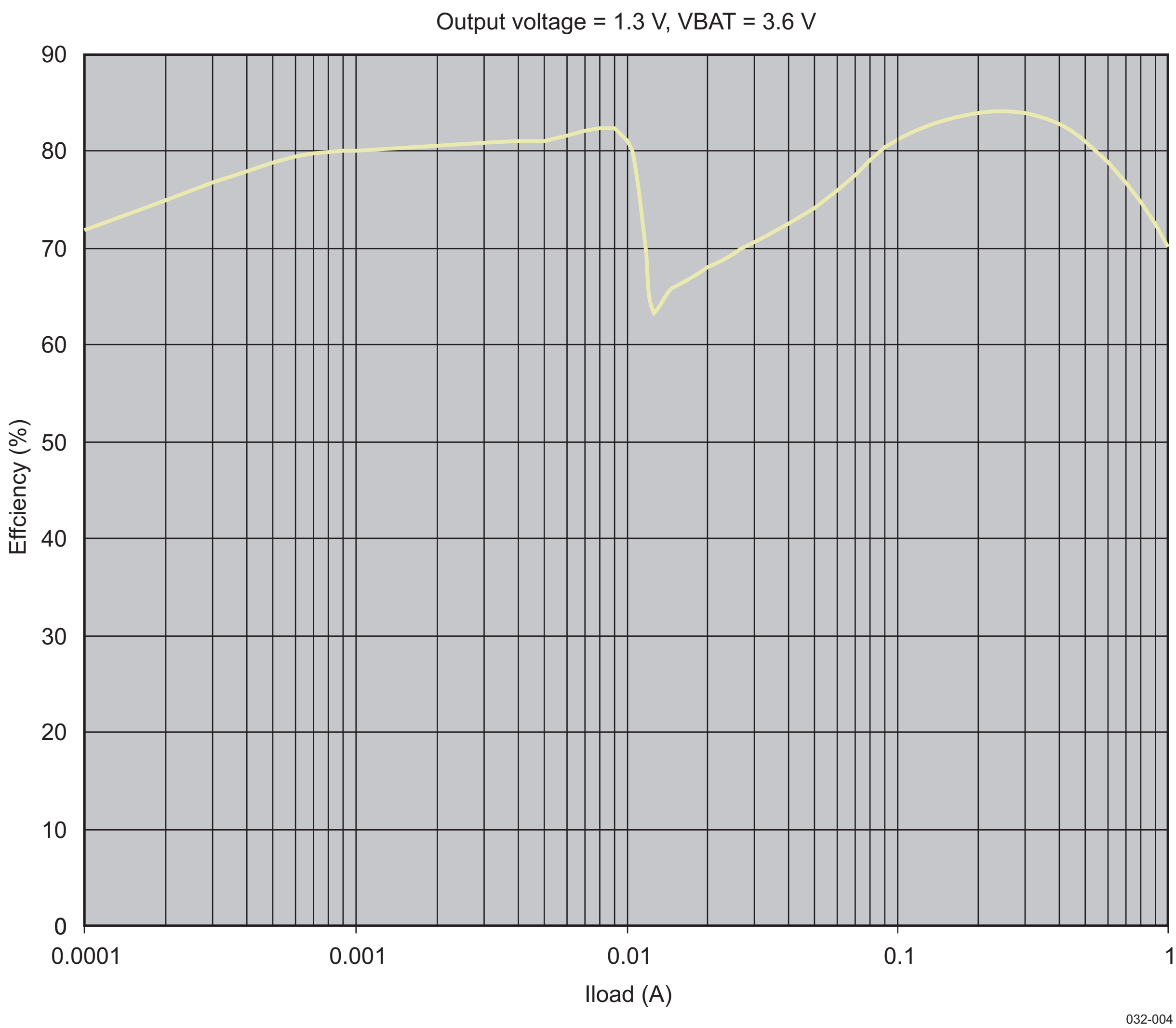


Figure 4-2. VDD1 dc-dc Regulator Efficiency

4.1.1.2 External Components and Application Schematic

Figure 4-3 is an application schematic with the external components on the VDD1 dc-dc regulator.

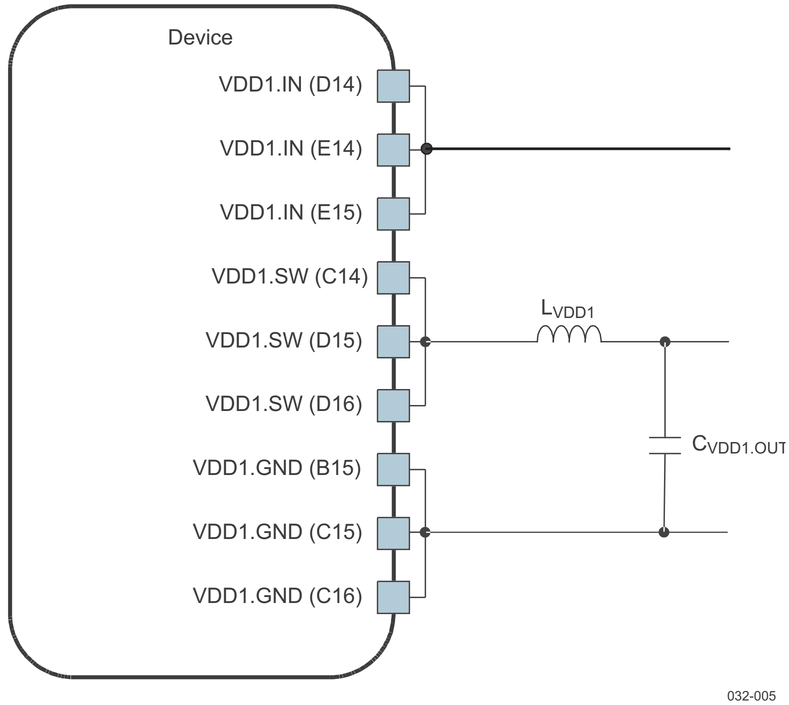


Figure 4-3. VDD1 dc-dc Application Schematic

NOTE

For the component values, see Table 15-1.

4.1.2 VDD2 dc-dc Regulator

4.1.2.1 VDD2 dc-dc Regulator Characteristics

The VDD2 dc-dc regulator is a programmable output stepdown dc-dc converter with an internal field effect transistor (FET). Like the VDD1 regulator, the VDD2 regulator can be placed in sleep or power-down mode and is SmartReflex-compatible. The VDD2 regulator differs from VDD1 in its current load capability. Table 4-4 lists the characteristics of the regulator.

Table 4-4. VDD2 dc-dc Regulator Characteristics

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage		0.6	1	1.5	V
Output voltage step	Covering the 0.6-V to 1.45-V range, 1.5 V is a single programmable value.		12.5		mV
Output accuracy(1)	0.6 to < 0.8 V	–6%		6%	
	0.8 o 1.5 V	–4%		4%	
Switching frequency			3.2		MHz
Conversion efficiency(2), Figure 4-4 in active mode and sleep mode	I_O = 10 mA, sleep		82%		
	100 mA < I_O < 300 mA		85%		
	300 mA < I_O < 500 mA		80%		
Output current	Active mode			700	mA
	Sleep mode			10	
Ground current (I_Q)	Off at 30°C			1	μA
	Sleep, unloaded			50	
	Active, unloaded, not switching			300	
Short-circuit current	$V_{IN} = V_{Max}$		1.2		A
Load regulation	$0 < I_O < I_{Max}$			20	mV
Transient load regulation(3)	I_O = 10 mA to (I_{Max}/2) + 10 mA, Maximum slew rate is I_{Max}/2/100 ns.	–65		50	mV
Line regulation				10	mV
Transient line regulation	300 mV_{PP} ac input, 10-μs rise and fall time			10	mV
Output shunt resistor (internal pulldown)			500	700	Ω
Startup time			0.25	1	ms
Recovery time	From sleep mode to on mode with constant load		25	100	μs
Slew rate (rising or falling)(4)		4	8	16	mV/μs
External coil	Value	0.7	1	1.3	μH
	DCR			0.1	Ω
	Saturation current	900			mA
External capacitor(5)	Value	8	10	12	μF
	ESR at switching frequency	0		20	mΩ

(1) Accuracy includes all variations (line and load regulations, line and load transients, temperature, and process)
(2) VBAT = 3.8 V, VDD2 = 1.3 V, Fs = 3.2 MHz, L = 1 μH, L_{DCR} = 100 mΩ, C = 10 μF, ESR = 10 mΩ
(3) Output voltage must discharge the load current completely and settle to its final value within 100 μs.
(4) Load current varies proportionally with the output voltage. The slew rate is for increasing and decreasing voltages and the maximum load current is 600 mA.
(5) Under current load condition step:
Imax/2 (300 mA) in 100 ns with a ±20% external capacitor accuracy or
Imax/3 (200 mA) in 100 ns with a ±50% external capacitor accuracy

See Table 2-2 for how to connect the VDD2 dc-dc converter when it is not used.

Figure 4-4 shows the efficiency of the VDD2 dc-dc regulator in active and sleep modes.

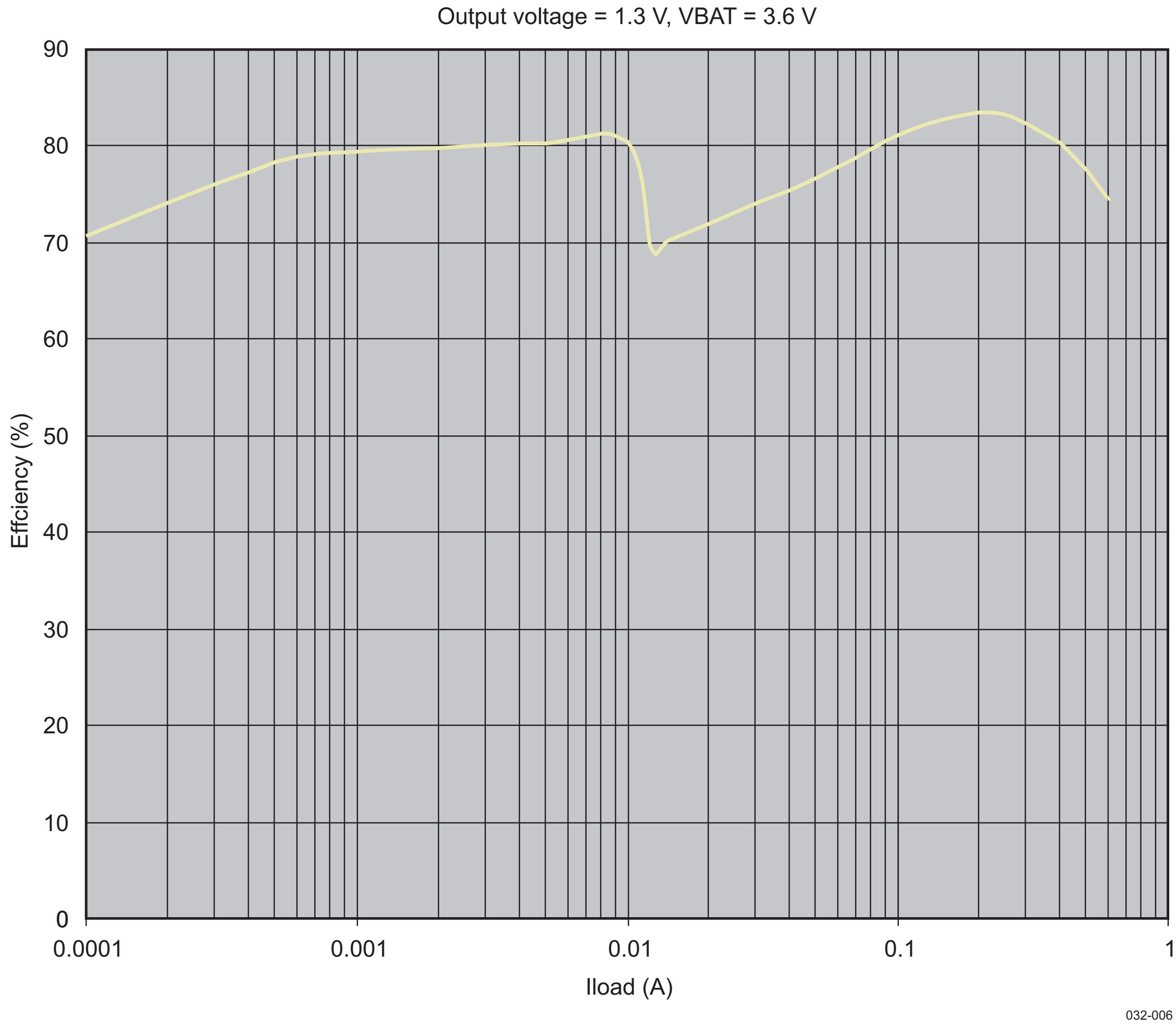


Figure 4-4. VDD2 dc-dc Regulator Efficiency

4.1.2.2 External Components and Application Schematic

Figure 4-5 is an application schematic with the external components of the VDD2 dc-dc regulator.

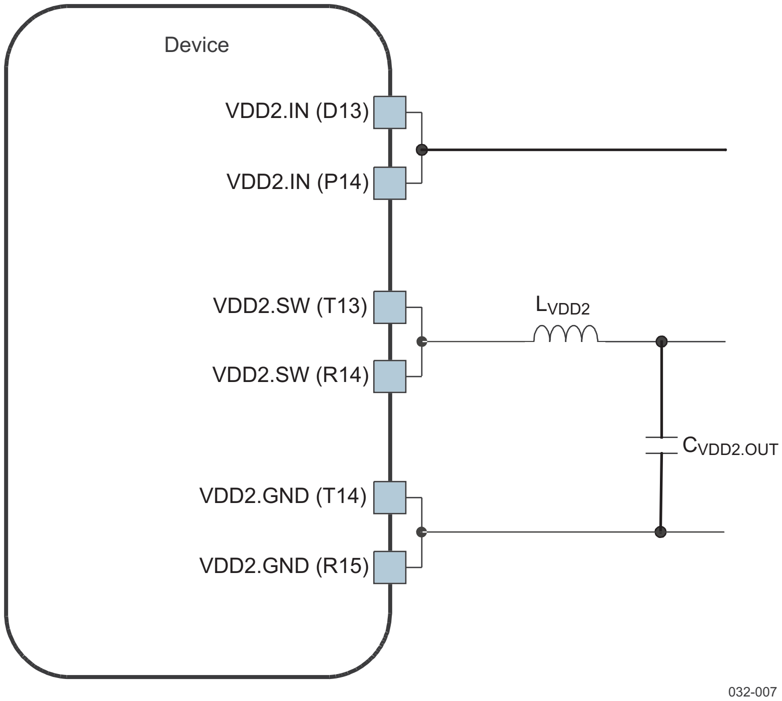


Figure 4-5. VDD2 dc-dc Application Schematic

NOTE

For the component values, see Table 15-1.

4.1.3 VIO dc-dc Regulator

4.1.3.1 VIO dc-dc Regulator Characteristics

The I/Os and memory dc-dc regulator is a 600-mA stepdown dc-dc converter (internal FET) with two output voltage settings. It supplies the memories and all I/O ports in the application and is one of the first power providers to switch on in the power-up sequence. This dc-dc regulator can be placed in sleep or power-down mode; however, care must be taken in the sequencing of this power provider, because numerous electrostatic discharge (ESD) blocks are connected to this supply. Table 4-5 lists the characteristics of the regulator.

Table 4-5. VIO dc-dc Regulator Characteristics

Parameter	Comments	Min	Typ	Max	Unit
Input voltage range		2.7	3.6	4.5	V
Output voltage(1)			1.8 1.85		V
Output accuracy (2)		–4%		4%	
		–3%		3%	
Switching frequency			3.2		MHz
Conversion efficiency(3) Figure 4-6 in active mode and sleep modes	I_O = 10 mA, sleep		85%		
	100 mA < I_O < 400 mA		85%		
	400 mA < I_O < 600 mA		80%		
Output current	On mode			700	mA
	Sleep mode			10	
Ground current (I_Q)	Off at 30°C			1	µA
	Sleep, unloaded			50	
	Active, unloaded, not switching			300	
Load transient(4)				50	mV
Line transient	300 mV_{PP} ac, input rise and fall time 10 µs			10	mV
Start-up time			0.25	1	ms
Recovery time	From sleep mode to on mode with constant load		<10	100	µs
Output shunt resistor (internal pulldown)			500	700	Ω
External coil	Value	0.7	1	1.3	µH
	DCR			0.1	Ω
	Saturation current	900			mA
External capacitor	Value	8	10	12	µF
	ESR at switching frequency	1		20	mΩ

(1) This voltage is tuned according to the platform and transient requirements.
(2) ±4% accuracy includes all variations (line and load regulation, line and load transient, temperature, process).
±3% accuracy is dc accuracy only.
(3) VBAT = 3.8 V, VIO = 1.8 V, Fs = 3.2 MHz, L = 1 µH, L_{DCR} = 100 mΩ, C = 10 µF, ESR = 10 mΩ
(4) Load transient can also be specified as 0 < I_O < I_{OUTmax}/2, Δt = 1 µs, 100 mV but this is not included in ±4% accuracy.

Figure 4-6 shows the efficiency of the VIO dc-dc regulator in active and sleep modes.

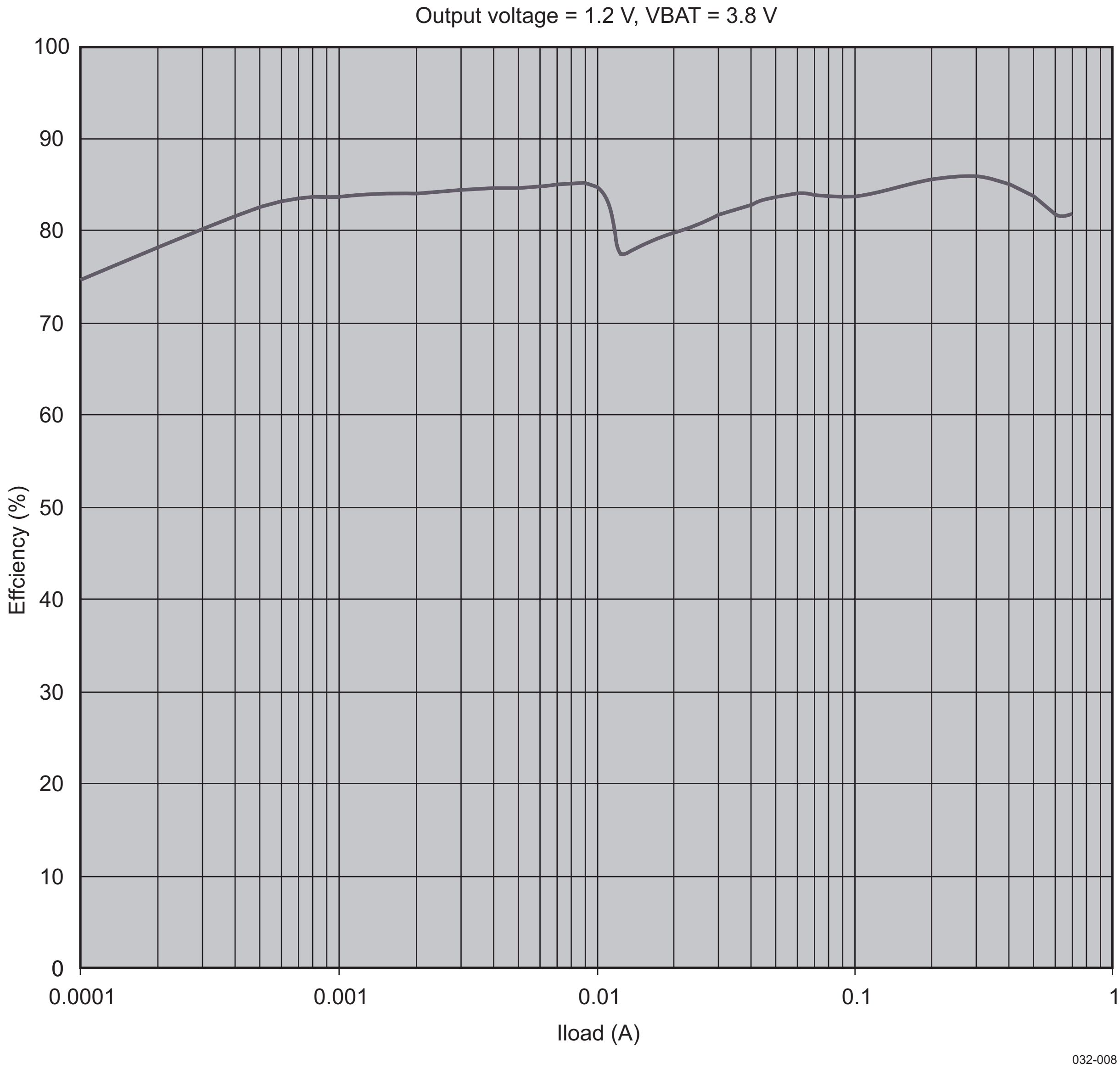


Figure 4-6. VIO dc-dc Regulator Efficiency in Active Mode

4.1.3.2 External Components and Application Schematic

Figure 4-7 is an application schematic with the external components of the VIO dc-dc regulator.

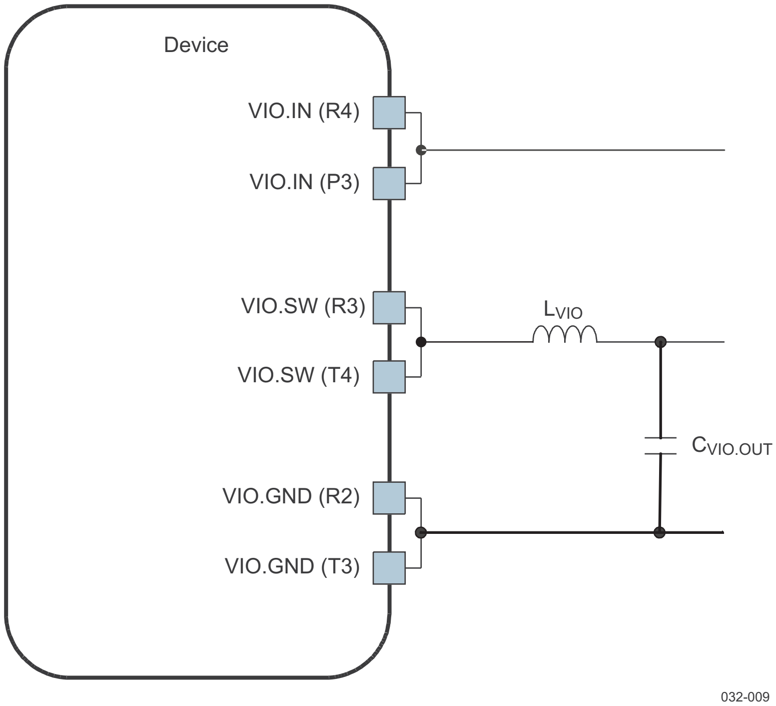


Figure 4-7. VIO dc-dc Application Schematic

NOTE

For the component values, see Table 15-1.

4.1.4 VDAC LDO Regulator

The VDAC programmable LDO regulator is a high power-supply ripple rejection (PSRR), low-noise, linear regulator that powers the host processor dual-video DAC. It is controllable with registers through I^2C and can be powered down. Table 4-6 lists the characteristics of the regulator.

Table 4-6. VDAC LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VDAC.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode	1.164	1.2	1.236	V
			1.261	1.3	1.339	
			1.746	1.8	1.854	
I_{OUT}	Rated output current	On mode			70	mA
		Low-power mode			5	
	dc load regulation	On mode: $0 < I_O < I_{Max}$			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 20 kHz	65			dB
		20 kHz < f < 100 kHz	45			
		f = 1 MHz	40			
		$V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$				
	Output noise	100 Hz < f < 5 kHz			400	nV/√Hz
		5 kHz < f < 400 kHz			125	
		400 kHz < f < 10 MHz			50	
	Ground current	On mode, $I_{OUT} = 0$			150	μA
		On mode, $I_{OUT} = I_{OUTmax}$			350	
		Low-power mode, $I_{OUT} = 0$			15	
		Low-power mode, $I_{OUT} = 1$ mA			25	
		Off mode at 55°C			1	
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: I_{Min} – I_{Max} Slew: 60 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV

4.1.5 VPLL1 LDO Regulator

The VPLL1 programmable LDO regulator is high-PSRR, low-noise, linear regulator used for the host processor phase-locked loop (PLL) supply. Table 4-7 lists the characteristics of the regulator.

Table 4-7. VPLL1 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VPLL1.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	0.97	1.0	1.03	V
			1.164	1.2	1.236	
			1.261	1.3	1.339	
			1.746	1.8	1.854	
			2.716	2.8	2.884	
			2.91	3.0	3.090	
I_{OUT}	Rated output current	On mode			40	mA
		Low-power mode			5	
	dc load regulation	On mode: $0 < I_O < I_{Max}$			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz	50			dB
		10 kHz < f < 100 kHz	40			
		f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	30			
	Ground current	On mode, $I_{OUT} = 0$			70	µA
		On mode, $I_{OUT} = I_{OUTmax}$			110	
		Low-power mode, $I_{OUT} = 0$			15	
		Low-power mode, $I_{OUT} = 1$ mA			16	
		Off mode at 55°C			1	
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: I_{Min} – I_{Max} Slew: 60 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV

4.1.6 VPLL2 LDO Regulator

The VPLL2 programmable LDO regulator is a high-PSRR, low-noise, linear regulator used for the host processor PLL supply. Table 4-8 lists the characteristics of the regulator.

Table 4-8. VPLL2 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VPLL2.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	0.672 0.97 1.164 1.261 1.455 1.746 1.795 2.425 2.522 2.716 2.765 2.91 3.05	0.7 1.0 1.2 1.3 1.5 1.8 1.85 2.5 2.6 2.8 2.85 3.0 3.15	0.728 1.03 1.236 1.339 1.545 1.854 1.906 2.575 2.678 2.884 2.936 3.09 3.245	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	dc load regulation	On mode: $0 < I_O < I_{Max}$			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			70 160 17 20 1	μA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: $I_{Min} – I_{Max}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV

4.1.7 VMMC1 LDO Regulator

The VMMC1 LDO regulator is a programmable linear voltage converter that powers the multimedia channel (MMC) slot. It includes a discharge resistor and overcurrent (short -ircuit) protection. This LDO regulator can also be turned off automatically when MMC card extraction is detected. The VMMC1 LDO can be powered through an independent supply other than the battery; for example, a charge pump (CP). In this case, the input from the VMMC1 LDO can be higher than the battery voltage. Table 4-9 lists the characteristics of the regulator.

Table 4-9. VMMC1 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VMMC1.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	5.5	V
V_{OUT}	Output voltage	On mode and low-power mode	1.7945 2.7645 2.91 3.0555	1.85 2.85 3.0 3.15	1.9055 2.9355 3.09 3.2445	V
I_{OUT}	Rated output current	On mode Low-power mode			220 5	mA
	dc load regulation	On mode: $0 < I_O < I_{Max}$			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 290 17 20 1	μA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: $I_{Min} – I_{Max}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV

4.1.8 VMMC2 LDO Regulator

The VMMC2 LDO regulator is a programmable linear voltage converter that powers MMC slot 2. It includes a discharge resistor and overcurrent (short-circuit) protection. The VMMC2 LDO can be powered through an independent supply other than the battery (for example, a CP). In this case, the input from the VMMC2 LDO can be higher than the battery voltage. Table 4-10 lists the characteristics of the regulator.

Table 4-10. VMMC2 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VMMC2.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	5.5	V
V_{OUT}	Output voltage	On mode and low-power mode	0.7 1.164 1.261 1.455 1.746 1.795 2.425 2.522 2.716 2.765 2.91 3.056	1.0 1.2 1.3 1.5 1.8 1.85 2.5 2.6 2.8 2.85 3.0 3.15	1.03 1.236 1.339 1.545 1.854 1.906 2.575 2.678 2.884 2.936 3.09 3.245	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	dc load regulation	On mode: $0 < I_O < I_{Max}$			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 50$ µA Off mode at 55°C			70 170 17 20 1	µA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: I_{Min} – I_{Max} Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV

4.1.9 VSIM LDO Regulator

The VSIM voltage regulator is a programmable, low-dropout, linear voltage regulator that supplies the subscriber identity module (SIM)-card and the SIM-card driver. This LDO regulator can be turned off automatically when SIM card extraction is detected. Table 4-11 lists the characteristics of the regulator.

Table 4-11. VSIM LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VSIM.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	0.97 1.164 1.261 1.746 2.716 2.91	1.0 1.2 1.3 1.8 2.8 3.0	1.03 1.236 1.339 1.854 2.884 3.09	V
I_{OUT}	Rated output current	On mode Low-power mode			50 1	mA
	dc load regulation	On mode: $0 < I_O < I_{Max}$			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT})			100	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 1$ mA Off mode at 55°C			70 120 15 16 1	µA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: $I_{Min} – I_{Max}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV

4.1.10 VAUX1 LDO Regulator

The VAUX1 GP LDO regulator powers the auxiliary devices. The VAUX1 regulator can also support an inductive load such as a vibrator. While operating in vibrator mode, the VAUX1 LDO has the following features:

- Programmable, register-controlled, soft-start function
- Enabled through the VIBRA.SYNC pin
- Programmable, register-controlled, duty cycle (PWM generator) based on a nominal 4-Hz cycle derived from an internal 32-kHz clock

Table 4-12 lists the characteristics of the regulator.

Table 4-12. VAUX1 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VAUX1.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
	Vibrator inductive load(1)	Connected from VAUX1.OUT to analog ground	70		700	µH
	Vibrator load resistance(1)		15		50	Ω
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	1.455 1.746 2.425 2.716 2.91	1.5 1.8 2.5 2.8 3.0	1.545 1.854 2.575 2.884 3.09	V
I_{OUT}	Rated output current	On mode Low-power mode			200 5	mA
	dc load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ µF (within 10% of V_{OUT}) Soft-start function for inductive load			100 500	µs
	Turn-off time				5000	µs
	Wake-up time	Full load capability			10	µs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 270 15 20 1	µA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: $I_{Min} – I_{Max}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV

(1) Parameter not tested, used for design specification only

4.1.11 VAUX2 LDO Regulator

The VAUX2 GP LDO regulator powers the auxiliary devices. Table 4-13 lists the characteristics of the regulator.

Table 4-13. VAUX2 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VAUX2.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	–3%	1.3 1.5 1.7 1.8 1.9 2.0 2.1 2.2 2.3 2.4 2.5 2.8	3%	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	dc load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 170 17 20 1	μA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: $I_{Min} – I_{Max}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV

4.1.12 VAUX3 LDO Regulator

The VAUX3 GP LDO regulator powers the auxiliary devices. Table 4-14 lists the characteristics of the regulator.

Table 4-14. VAUX3 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VAUX3.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	1.455 1.746 2.425 2.716 2.91	1.5 1.8 2.5 2.8 3.0	1.545 1.854 2.575 2.884 3.09	V
I_{OUT}	Rated output current	On mode Low-power mode			200 5	mA
	dc load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 25			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 270 15 20 1	μA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: $I_{Min} – I_{Max}$ Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV

4.1.13 VAUX4 LDO Regulator

The VAUX4 GP LDO regulator powers the auxiliary devices. The VAUX4 regulator has an independent supply input pin and can be preregulated by an external voltage. Table 4-15 lists the characteristics of the regulator.

Table 4-15. VAUX4 LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VAUX4.OUT to analog ground	0.3	1	2.7	μF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage		2.7	3.6	4.5	V
V_{OUT}	Output voltage	On mode and low-power mode	0.672 0.97 1.164 1.261 1.455 1.746 1.795 2.425 2.522 2.716 2.765 2.91 3.056	0.7 1.0 1.2 1.3 1.5 1.8 1.85 2.5 2.6 2.8 2.85 3.0 3.15	0.728 1.03 1.236 1.339 1.545 1.854 1.906 2.575 2.678 2.884 2.936 3.09 3.245	V
I_{OUT}	Rated output current	On mode Low-power mode			100 5	mA
	dc load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			20	mV
	dc line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			3	mV
	Turn-on time	$I_{OUT} = 0$, $C_L = 1$ μF (within 10% of V_{OUT})			100	μs
	Wake-up time	Full load capability			10	μs
	Ripple rejection	f < 10 kHz 10 kHz < f < 100 kHz f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{Max}$	50 40 30			dB
	Ground current	On mode, $I_{OUT} = 0$ On mode, $I_{OUT} = I_{OUTmax}$ Low-power mode, $I_{OUT} = 0$ Low-power mode, $I_{OUT} = 5$ mA Off mode at 55°C			70 170 17 20 1	μA
V_{DO}	Dropout voltage	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{Load}: I_{Min} – I_{Max} Slew: 40 mA/μs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/μs			10	mV

4.1.14 Internal LDOs

Table 4-16 lists the regulators that power the device, and the output loads associated with them.

Table 4-16. Output Load Conditions

Regulator	Parameter	Test Conditions	Min	Typ	Max	Unit
VINTDIG LDO	Filtering capacitor	Connected from VINTDIG.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
VINTANA1 LDO	Filtering capacitor	Connected from VINTANA1.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
VINTANA2 LDO	Filtering capacitor	Connected from VINTANA2.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
VRUSB_3V1 LDO	Filtering capacitor	Connected from VUSB.3P1 to GND	0.3	1	2.7	µF
	Filtering capacitor ESR		0	10	600	mΩ
VRUSB_1V8 LDO	Filtering capacitor	Connected from VINTUSB1P8.OUT to GND	0.3	1	2.7	µF
	Filtering capacitor ESR		0	10	600	mΩ
VRUSB_1V5 LDO	Filtering capacitor	Connected from VINTUSB1P5 to GND	0.3	1	2.7	µF
	Filtering capacitor ESR		0	10	600	mΩ

4.1.15 CP

The CP generates a 4.8-V (nominal) power supply voltage from the battery to the VBUS pin. The input voltage range is 2.7 to 4.5 V for the battery voltage. The CP operating frequency is 1 MHz.

The CP tolerates 7 V on VBUS when it is in power-down mode. The CP integrates a short-circuit current limitation at 450 mA. Table 4-17 lists the characteristics of the CP.

Table 4-17. CP Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VBUS to VSSP	1.41	4.7	6.5	µF
	Flying capacitor	Connected from CP to CN	1.32	2.2	3.08	µF
	Filtering capacitor ESR				20	mΩ
Electrical Characteristics						
V_{IN}	Input voltage	On mode: V_{IN} = VBAT	2.7	3.6	4.5	V
V_O	Output voltage		4.6	4.8	5.25	V
I_{load}	Rated output current	VBAT > 3 V at VBUS	0		100	mA
		2.7 V < VBAT < 3 V, at VBUS	0		50	
	Efficiency	I_{Load} = 100 mA, VBAT = 3.6 V		55%		
	Setting time	$I_{LOADmax/2}$ to I_{LOAmax} in 5 µs		100	400	µs
	Startup time				3	ms
	Short-circuit limitation current		250	350	450	mA
	dc load regulation	$I_{LOADmin}$ to $I_{LOADmax}$		250	500	mV
	dc line regulation	3.0 V to $VBAT_{max}$ I_{Load} = 100 mA		250	350	mV
	Transient load regulation	$I_{VBUS_5Vmax/2}$ – I_{VBUS_5Vmax} 50 µs, C = 2*4.7 µF		300	350	mV
		0 – $I_{VBUS_5Vmax/2}$, 50 µs, C = 2*4.7 µF			350	
	Transient line regulation	$VBAT_{min}$ to $VBAT_{max}$ in 50 µs, C = 2*4.7 µF		300	350	mV

4.1.16 USB LDO Short-Circuit Protection Scheme

The short-circuit current for the LDOs and dc-dc converters in TPS65950 is approximately twice the maximum load current. In certain cases when the output of the block is shorted to ground, the power dissipation can exceed the 1.2-W requirement if no action is taken. A short-circuit protection scheme is included in the TPS65950 to ensure that if the output of an LDO or dc-dc is short-circuited, the power dissipation does not exceed the 1.2-W level.

The three USB LDOs, VRUSB3V1, VRUSB1V8, and VRUSB1V5, are included in this short-circuit protection scheme, which monitors the LDO output voltage at a frequency of 1 Hz and generates an interrupt (sc_it) when a short circuit is detected.

The scheme compares the LDO output voltage to a reference voltage and detects a short circuit if the LDO voltage drops below this reference value (0.5 or 0.75 V programmable). In the case of the VRUSB3V1 and VRUSB1V8 LDOs, the reference is compared with a divided-down voltage (1.5 V typical).

If a short circuit is detected on VRUSB3V1, the power subchip FSM switches this LDO to sleep mode.

If a short circuit is detected on VRUSB1V8 or VRUSB1V5, the power subchip FSM switches off the relevant LDO.

4.2 Power References

The bandgap voltage reference is filtered (resistance/capacitance [RC] filter) using an external capacitor connected across the VREF output and an analog ground (REFGND). The VREF voltage is scaled, distributed, and buffered in the device. The bandgap is started in fast mode (not filtered), and is set automatically by the D machine in slow mode (filtered, less noisy) when required.

Table 4-18 lists the characteristics of the voltage references.

Table 4-18. Voltage Reference Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Condition						
	Filtering capacitor	Connected from V_{REF} to REFGND	0.3	1	2.7	μF
Electrical Characteristics						
V_{IN}	Input voltage	On mode	2.7	3.6	4.5	V
	Internal bandgap reference voltage	On mode, measured through TESTV terminal	1.272	1.285	1.298	V
	Reference voltage (V_{REF} terminal)	On mode	0.725	0.75	0.7575	V
	Retention mode reference	On mode	0.492	0.5	0.508	V
	I_{REF} NMOS sink		0.9	1	1.1	μA
	Ground current	Bandgap IREF block Preregulator VREF buffer Retention reference buffer			25 20 15 10 10	μA
	Output spot noise	100 Hz			1	μV/√Hz
	A-weighted noise (rms)			200		nV (ms)
	P-weighted noise (rms)			150		nV (ms)
	Integrated noise	20 Hz to 100 kHz		2.2		μV
	I_{BIAS} trim bit LSB				0.1	μA
	Ripple rejection	< 1 MHz from VBAT	60			dB
	Start-up time				1	ms

4.3 Power Control

4.3.1 Backup Battery Charger

If the backup battery is rechargeable, it can be recharged from the main battery. A programmable voltage regulator powered by the main battery allows recharging of the backup battery. The backup battery charge must be enabled using a control bit register. Recharging starts when two conditions are met:

- Main battery voltage > backup battery voltage
- Main battery > 3.2 V

The comparators of the backup battery system (BBS) give the two thresholds of the backup battery charge startup. The programmed voltage for the charger gives the end-of-charge threshold. The programmed current for the charger gives the charge current.

Overcharging is prevented by measurement of the backup battery voltage through the GP ADC. Table 4-19 lists the characteristics of the backup battery charger.

Table 4-19. Backup Battery Charger Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
VBACKUP-to-MADC input attenuation	VBACKUP from 1.8 to 3.3 V		0.33		V/V
Backup battery charging current	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 00	10	25	45	μA
	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 01	105	150	270	μA
	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 10	350	500	900	μA
	VBACKUP = 2.8 V, BBCHEN = 1, BBISEL = 11	0.7	1	1.8	mA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 00	17.5	25	45	μA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 01	105	150	270	μA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 10	350	500	900	μA
	VBACKUP = 0 V, BBCHEN = 1, BBISEL = 11	0.7	1	1.8	mA
End backup battery charging voltage: VBBCHGEND	$I_{VBACKUP}$ = –10 μA, BBSEL = 00	2.4	2.5	2.6	V
	$I_{VBACKUP}$ = –10 μA, BBSEL = 01	2.9	3.0	3.1	V
	$I_{VBACKUP}$ = –10 μA, BBSEL = 10	3.0	3.1	3.2	V
	$I_{VBACKUP}$ = –10 μA, BBSEL = 11	3.1	3.2	3.3	V

4.3.2 Battery Monitoring and Threshold Detection

4.3.2.1 Power On/Power Off and Backup Conditions

Table 4-20 lists the threshold levels of the battery.

Table 4-20. Battery Threshold Levels

Parameter	Test Conditions	Min	Typ	Max	Unit
Main battery charged threshold VMBCH	Measured on VBAT terminal	3.1	3.2	3.3	V
Main battery low threshold VMBLO	VBACKUP = 3.2 V, measured on VBAT terminal (monitored on terminal ONNOFF)	2.55	2.7	2.85	V
Main battery high threshold VMBHI	Measured on terminal VBAT, VBACKUP = 0 V Measured on terminal VBAT, VBACKUP = 3.2 V	2.5 2.5	2.65 2.85	2.95 2.95	V
Batteries not present threshold VBNPR	Measured on terminal VBACKUP with VBAT < 2.1 V Measured on terminal VBAT with VBACKUP = 0 V (monitored on terminal VRRTC)	1.6 1.95	1.8 2.1	2.0 2.25	V

4.3.3 VRRTC LDO Regulator

The VRRTC voltage regulator is a programmable, low dropout, linear voltage regulator supplying (1.5 V) the embedded real-time clock (32.768-kHz oscillator) and dedicated I/Os of the digital host counterpart. The VRRTC regulator is also the supply voltage of the power-management digital state-machine. The VRRTC regulator is supplied from the UPR line, switched on by the main or backup battery, depending on the system state. The VRRTC output is present as long as a valid energy source is present. The VRRTC line is supplied by an LDO when VBAT > 2.7, and a clamp circuit when in backup mode. Table 4-21 describes the regulator characteristics.

Table 4-21. VRRTC LDO Regulator Characteristics

Parameter		Test Conditions	Min	Typ	Max	Unit
Output Load Conditions						
	Filtering capacitor	Connected from VRTC.OUT to analog ground	0.3	1	2.7	µF
	Filtering capacitor ESR		20		600	mΩ
Electrical Characteristics						
V_{IN}	Input voltage	On mode	2.7	VBAT	4.5	V
V_{OUT}	Output voltage	On mode	1.45	1.5	1.55	V
I_{OUT}	Rated output current	On mode			30	mA
		Sleep mode			1	
	DC load regulation	On mode: $I_{OUT} = I_{OUTmax}$ to 0			100	mV
	DC line regulation	On mode, $V_{IN} = V_{INmin}$ to V_{INmax} at $I_{OUT} = I_{OUTmax}$			100	mV
	Turn-on time	$I_{OUT} = 0$, at $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
	Wake-up time	On mode from low power to On mode, $I_{OUT} = 0$, at $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		µs
		From backup to On mode, $I_{OUT} = 0$, at $V_{OUT} = V_{OUTfinal} \pm 3\%$		100		
	Ripple rejection (VRRTC)	f < 10 kHz	50			dB
		10 kHz < f < 100 kHz	40			
		f = 1 MHz $V_{IN} = V_{OUT} + 1$ V, $I_O = I_{MAX}$	30			
	Ground current	On mode, $I_{OUT} = 0$			70	µA
		On mode, $I_{OUT} = I_{OUTmax}$			100	
		Sleep mode, $I_{OUT} = 0$			10	
		Sleep mode, $I_{OUT} = 1$ mA			11	
		Off mode			1	
V_{DO}	Dropout voltage (1)	On mode, $I_{OUT} = I_{OUTmax}$			250	mV
	Transient load regulation	I_{LOAD}: $I_{MIN} – I_{MAX}$ Slew: 40 mA/µs	–40		40	mV
	Transient line regulation	V_{IN} drops 500 mV Slew: 40 mV/µs			10	mV
	Overshoot	Softstart			3%	
	Pull down resistance	Default in off mode	250	320	450	Ω

(1) For nominal output voltage

4.4 Power Consumption

Table 4-22 describes the power consumption, depending on the use cases.

NOTE

Typical power consumption is obtained in nominal operating conditions with the TPS65950 in stand-alone mode.

Table 4-22. Power Consumption

Mode	Description		Typical Consumption
Backup	Only the RTC date is maintained with a couple of registers in the backup domain. No main source is connected. Consumption is on the backup battery.	VBAT not present	2.25 * 3.2 = 7.2 μW
Wait-on	The phone is apparently off for the user, a main battery is present and well-charged. The RTC registers (registers in the backup domain) are maintained. Wake-up capabilities (like the PWRON button) are available.	VBAT = 3.8 V	64 * 3.8 = 243.2 μW
Active No Load	The subsystem is powered by the main battery, all supplies are enabled with full current capability, internal reset is released, and the associated processor is running.	VBAT = 3.8 V	3291 * 3.8 = 12505 μW
Sleep No Load	The main battery powers the subsystem, selected supplies are enabled but in low-consumption mode, and the associated processor is in low-power mode.	VBAT = 3.8 V	496 * 3.8 = 1884.4 μW

Table 4-23 lists the regulator states for each mode.

Table 4-23. Regulator States Depending on Use Cases

Regulator	Mode			
	Backup	Wait-On	Sleep No Load	Active No Load
VAUX1	OFF	OFF	OFF	OFF
VAUX2	OFF	OFF	SLEEP	ON
VAUX3	OFF	OFF	OFF	OFF
VAUX4	OFF	OFF	SLEEP	ON
VMMC1	OFF	OFF	OFF	OFF
VMMC2	OFF	OFF	SLEEP	ON
VPLL1	OFF	OFF	SLEEP	ON
VPLL2	OFF	OFF	SLEEP	ON
VSIM	OFF	OFF	OFF	OFF
VDAC	OFF	OFF	OFF	OFF
VINTANA1	OFF	OFF	SLEEP	ON
VINTANA2	OFF	OFF	SLEEP	ON
VINTDIG	OFF	OFF	SLEEP	ON
VIO	OFF	OFF	SLEEP	ON
VDD1	OFF	OFF	SLEEP	ON
VDD2	OFF	OFF	SLEEP	ON
VUSB_1V5	OFF	OFF	OFF	OFF
VUSB_1V8	OFF	OFF	OFF	OFF
VUSB_3V1	OFF	OFF	SLEEP	SLEEP

4.5 Power Management

4.5.1 Boot Modes

The modes corresponding to the BOOT0–BOOT1 combination value are listed in Table 4-24.

Table 4-24. BOOT Mode Description

Name	Description	BOOT0	BOOT1
	Reserved	0	0
MC027	Master_C027_Generic 01	0	1
MC021	Master_C021_Generic 10	1	0
SC021	Slave_C021_Generic 11	1	1

4.5.2 Process Modes

The process modes parameter defines:

- The boot voltage for the host core
- The boot sequence associated with the process
- The dynamic voltage and frequency scaling (DVFS) protocol associated with the process

4.5.2.1 C027.0 Mode

Table 4-25 lists the parameters for C027.0 mode.

Table 4-25. C027.0 Mode Description

Boot core voltage	1.3 V
Power sequence	VIO followed by VDD1 and VPLL
DVFS protocol	VMODE1/2

4.5.2.2 C021.M Mode

Table 4-26 lists the parameters for C021.M mode.

Table 4-26. C021.M Mode Description

Boot core voltage	1.2 V
Power sequence	VIO followed by VPLL1, VDD2, VDD1
DVFS protocol	SmartReflex IF (I^2C high speed)

4.5.3 Power-On Sequence

4.5.3.1 Timings Before Sequence_Start

The starting time of the power-on sequence relative to external events is shown in Figure 4-8.

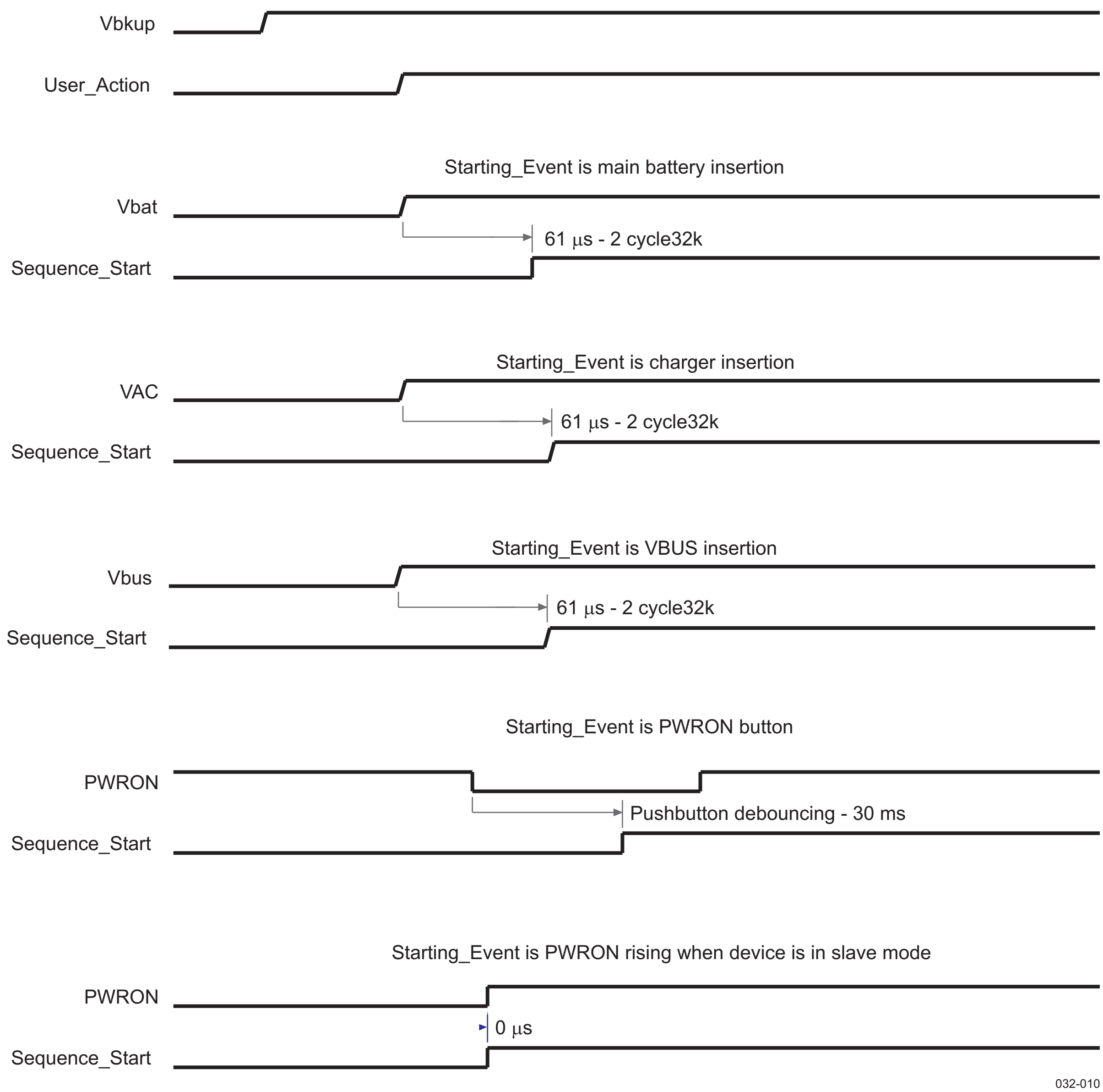


Figure 4-8. Timings Before Sequence Start

4.5.3.2 OMAP2 Power-On Sequence

Figure 4-9 shows the timing and control that must occur in Master_C027_Generic mode. Sequence_Start occurs according to the events shown in Figure 4-8.

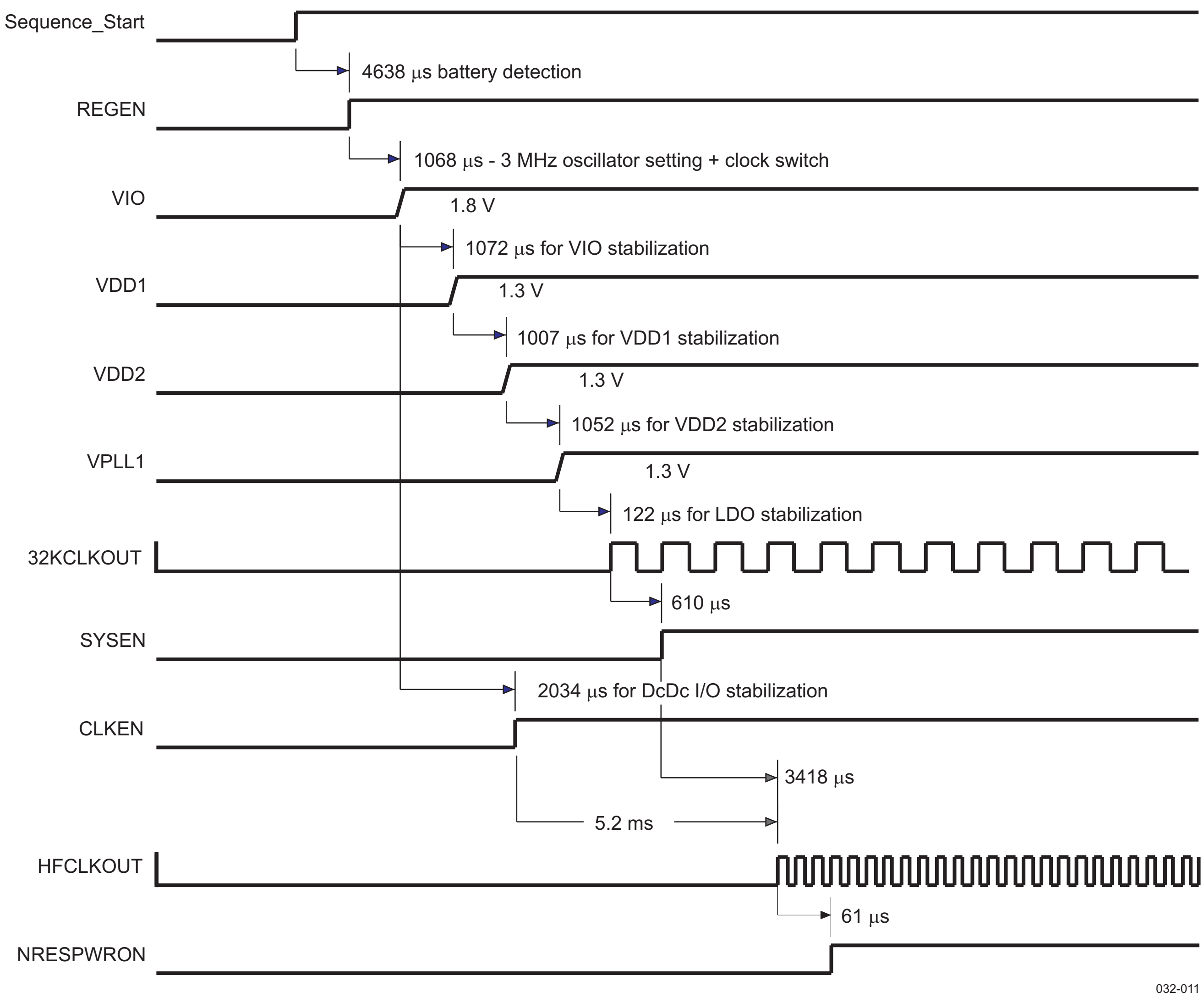


Figure 4-9. Timings—OMAP2 Power-On Sequence

4.5.3.3 OMAP3 Power-On Sequence

Figure 4-10 shows the timing and control that must occur in Master_C021_Generic mode. Sequence_Start occurs according to the events shown in Figure 4-8.

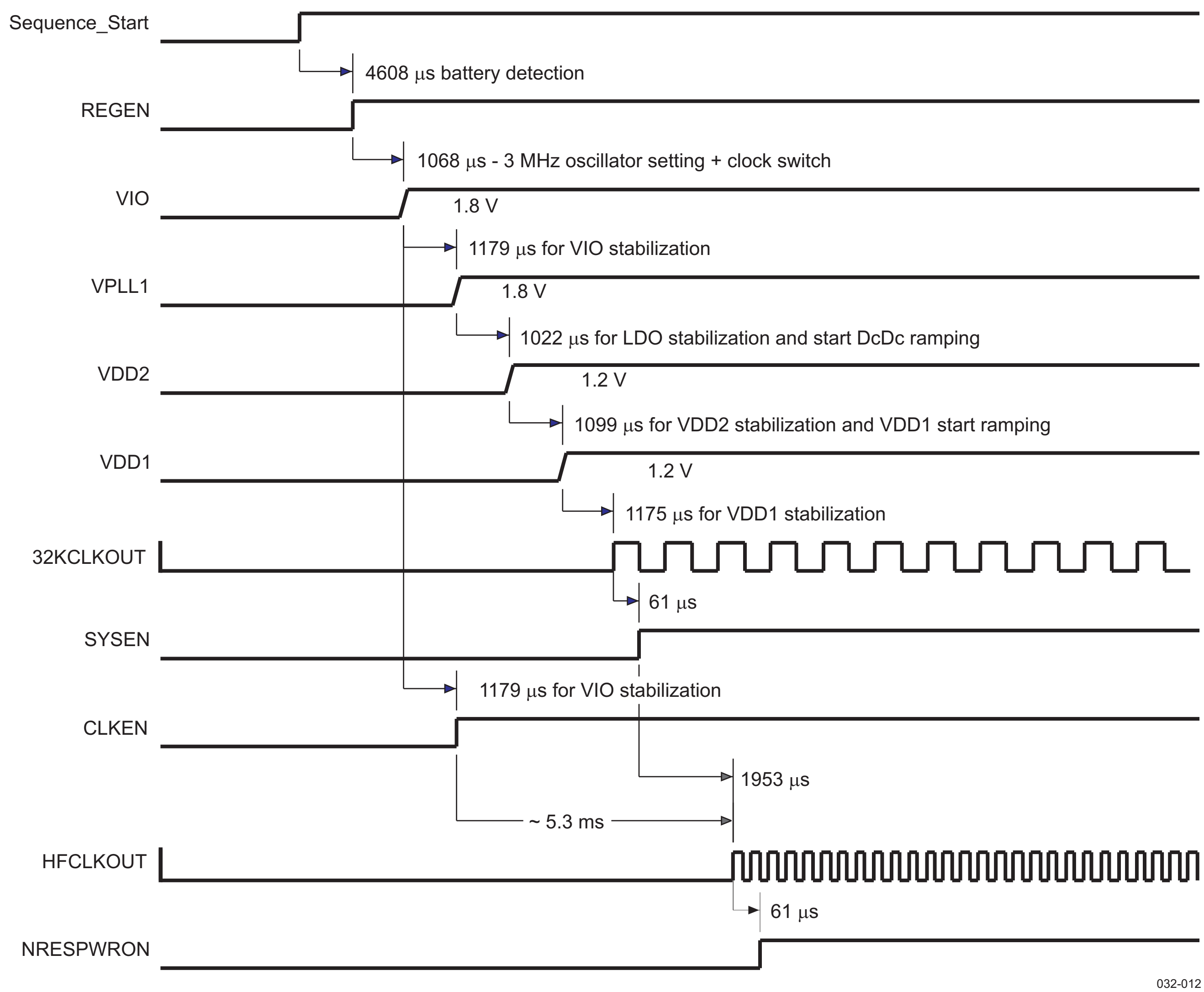


Figure 4-10. Timings—OMAP3 Power-On Sequence

4.5.3.4 Power On in Slave_C021_Generic Mode

Figure 4-11 describes the timing and control that must occur in the Slave_C021_Generic mode. Sequence_Start is a symbolic internal signal to ease the description of the power sequences and occurs according to the different events detailed in Figure 4-8.

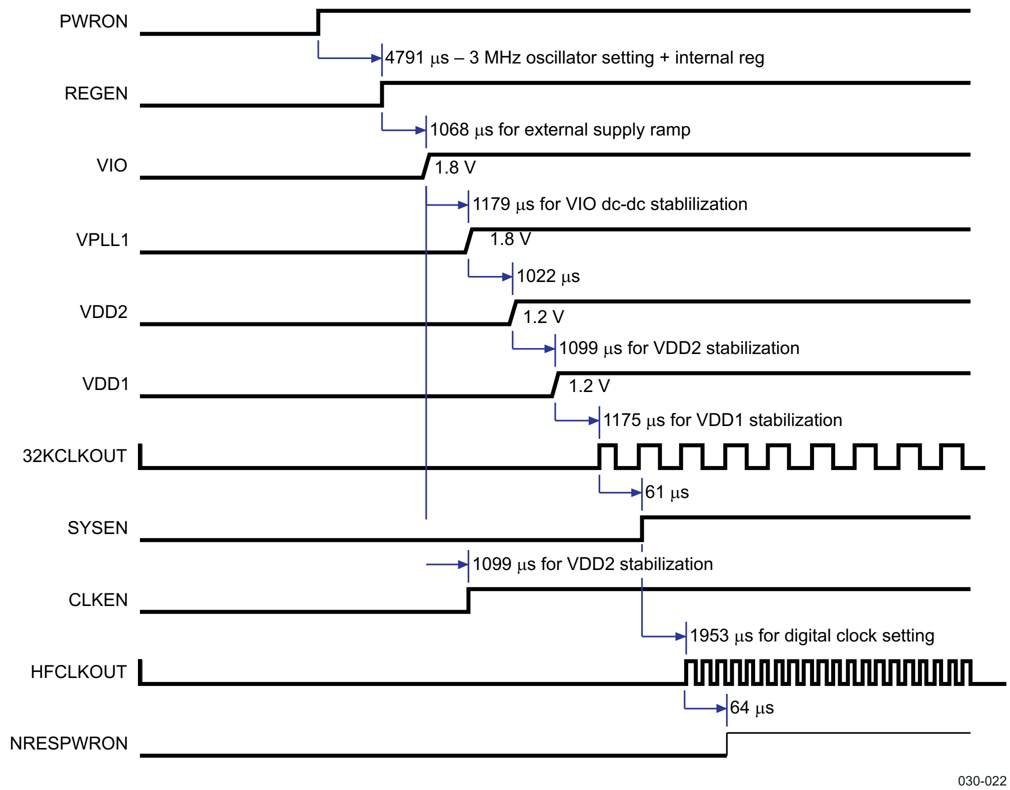


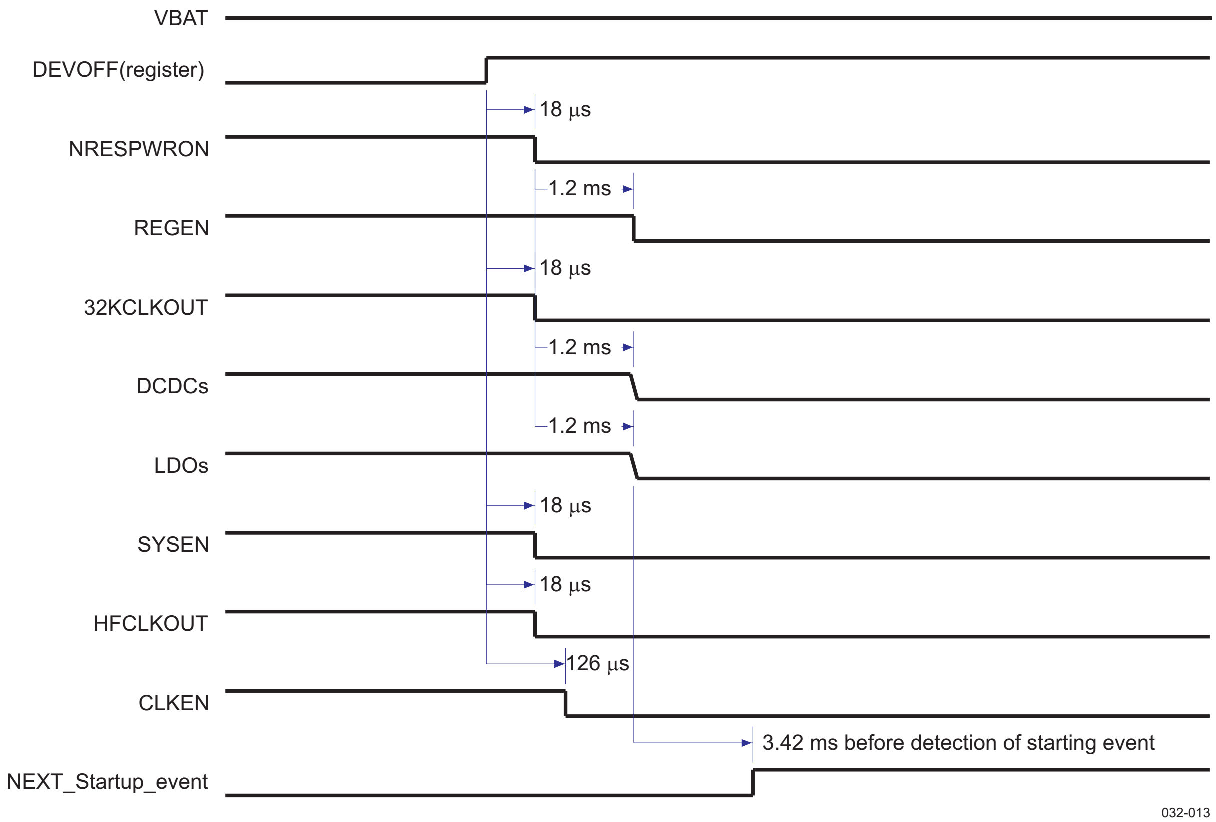
Figure 4-11. Timings—Power On in Slave_C021_Generic Model

4.5.4 Power-Off Sequence

This section describes the signal behavior required to power down the system.

4.5.4.1 Power-Off Sequence in Master Modes

Figure 4-12 shows the timing and control that occur during the power-off sequence in master modes.



NOTE: All timings are typical values with the default setup (depending on the resynchronization between power domains, state machinery priority, etc.).

Figure 4-12. Power-Off Sequence in Master Modes

If the value of the HF clock is not 19.2 MHz (with the values of the CFG_BOOT HFCLK_FREQ bit field set accordingly), the delay between DEVOFF and NRESPWRON/CLK32KOUT/SYSEN/HFCLKOUT is divided by two (approximately 9 µs). This is caused by the internal frequency used by power STM switching from 3 to 1.5 MHz if the HF clock value is 19.2 MHz.

The DEVOFF event is PWRON falling edge in slave mode and DEVOFF internal register write in master mode.

5 Real-Time Clock and Embedded Power Controller

The TPS65950 device contains an RTC to provide clock and timekeeping functions and an EPC to provide battery supervision and control.

5.1 RTC

The RTC provides the following basic functions:

- Time information (seconds/minutes/hours) directly in binary-coded decimal (BCD) code
- Calendar information (day/month/year/day of the week) directly in BCD code
- Interrupt generation periodically (1 second/1 minute/1 hour/1 day) or at a precise time (alarm function)
- 32-kHz oscillator drift compensation and time correction
- Alarm-triggered system wake-up event

5.1.1 Backup Battery

The TPS65950 implements a backup mode in which a backup battery can keep the RTC running to maintain clock and time information even if the main supply is not present. If the backup battery is rechargeable, the device also provides a backup battery charger so it can be recharged when the main battery supply is present.

The backup domain powers the following:

- Internal 32.768-kHz crystal oscillator
- RTC
- Eight GP storage registers
- Backup domain low-power regulator (VBRTC)

5.2 EPC

The EPC provides five system states for optimal power use by the system, as listed in Table 5-1.

Table 5-1. System States

System State	Description
NO SUPPLY	The system is not powered by any battery.
BACKUP	The system is powered only with the backup battery and maintains only the VBRTC supply.
WAIT-ON	The system is powered by the main battery and maintains only the VRRTC supply. It can accept switch-on requests.
ACTIVE	The system is powered by the main battery; all supplies can be enabled with full current capability.
SLEEP	The main battery powers the system; selected supplies are enabled, but in low consumption mode.

Three categories of events can trigger state transitions:

- Hardware events: Supply/battery insertion, wake-up requests, USB plug, and RTC alarm
- Software events: Switch-off commands, switch-on commands, and sleep-on commands
- Monitoring events: Supply/battery level check, main battery removal, main battery fail, and thermal shutdown

6 Audio/Voice Module

The audio codec in the device includes five DACs and two ADCs to provide multiple voice channels and stereo downlink channels that can support all standard audio sample rates through I2S/TDM format interfaces. The audio output stages on the device include stereo headset amplifiers, two integrated class-D amplifiers providing stereo differential outputs, predrivers for line outputs, and an earpiece amplifier. The input audio stages include three differential microphone inputs, stereo line inputs, and interface for digital micrphones. Automatic and programmable gain control is available with all necessary digital filtering, side-tone functions, and pop-noise reduction.

Figure 6-1 is a block diagram of the audio/voice module.

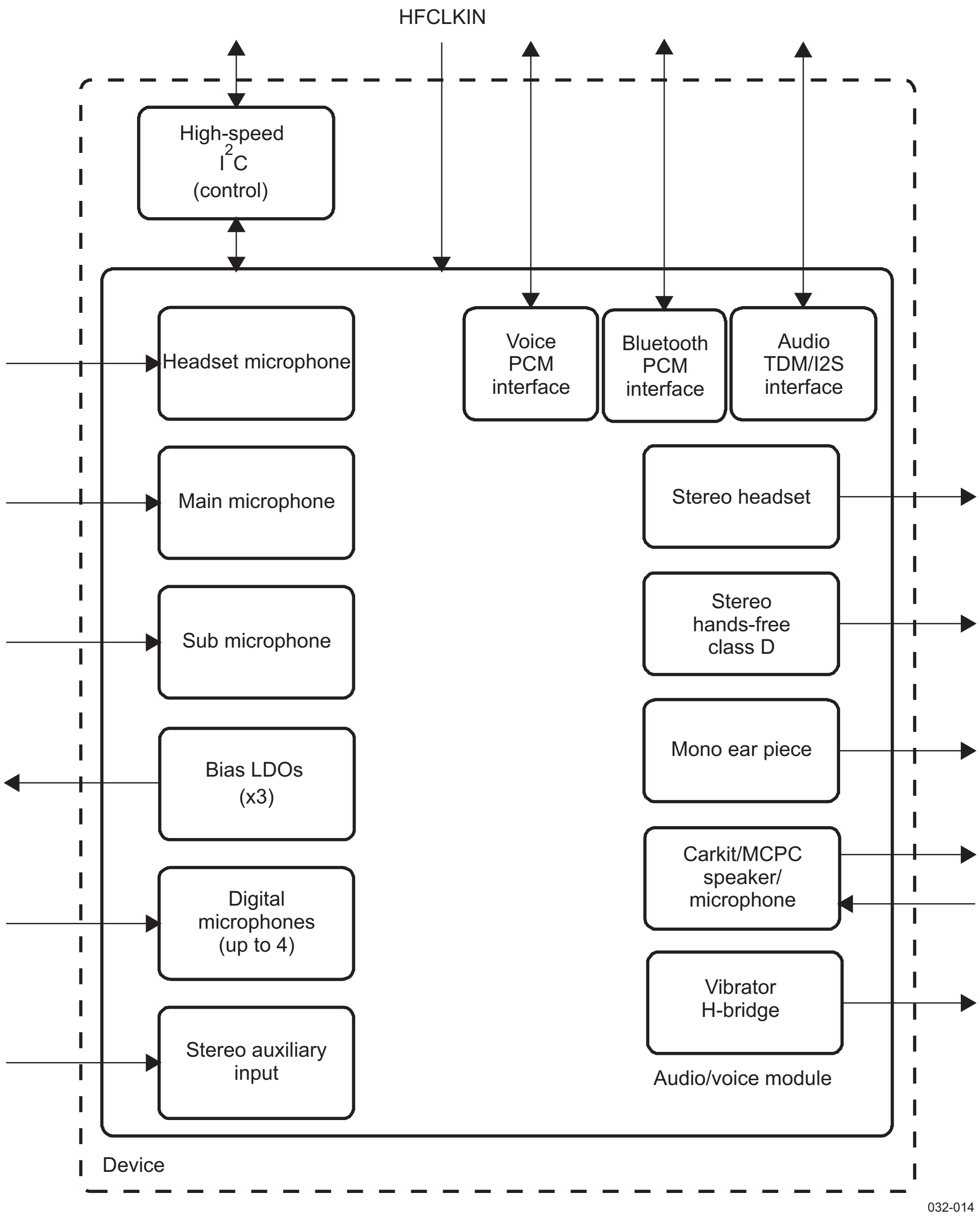


Figure 6-1. Audio/Voice Module Block Diagram

6.1 Audio/Voice Downlink (RX) Module

The audio/voice module includes the following output stages:

- Mono/stereo single-ended headset amplifier
- Stereo differential integrated class-D 8-Ω hands-free amplifiers
- Predriver output signals for external class-D amplifiers (single-ended)
- Mono differential earpiece amplifier
- Vibrator H-bridge

6.1.1 Earphone Output

6.1.1.1 Earphone Output Characteristics

Analog signals from the audio and/or voice interface are fed to the earphone amplifier. This amplifier, with different gains, provides a full differential signal on terminals EARP and EARM. Figure 6-2 shows the earphone amplifier. Table 6-1 lists the output characterstics of the earphone amplifier.

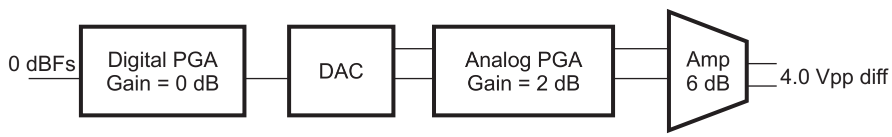


Figure 6-2. Earphone Amplifier

Table 6-1. Earphone Amplifier Output Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Differential load impedance		26	32		Ω
		100	100		pF
Gain range (1)	Audio path	–86		36	dB
	Voice path	–60		36	
Absolute gain error		–1		1	dB
Maximum output power	At 1.4 Vrms differential output voltage Load impedance = 32 Ω		61.25		mW
Peak-to-peak differential output voltage (0 dBFs)	Default gain (2)		4.0		V_{PP}
Total harmonic distortion Default gain (2) Load impedance = 32 Ω	At 0 dBFs		–65	–60	dB
	At –6 dBFs		–70	–65	
	At –20 dBFs			–60	
	At –60 dBFs			–30	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Gain = 0 dB Load = 32 Ω		–90	–85	dBFs
Output PSRR (for all gains)	20 Hz to 4 kHz		90		dB
	20 Hz to 20 kHz		70		

(1) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps)
Voice digital filter = –36 to 12 dB (1-dB steps)
ARXPGA (volume control) = –24 to 12 dB (2-dB steps)
Output driver = 0, 6, 12 dB
(2) The default gain setting assumes the ARXPGA has 2-dB gain setting (volume control) and output driver at 6-dB gain setting.

6.1.1.2 External Components and Application Schematic

Figure 6-3 is a simplified schematic of the earphone speaker.

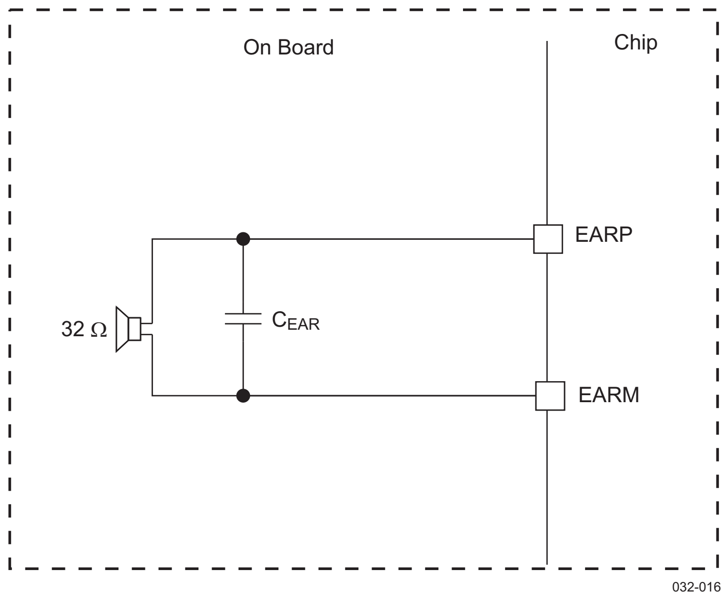


Figure 6-3. Earphone Speaker

NOTE

For the component values, see Table 15-1.

6.1.2 8-Ω Stereo Hands-Free

The digital signal from the audio and/or voice interface is fed to two class-D amplifiers. These 8-Ω speaker amplifiers provide a stereo differential signal on terminal pairs (IHF.RIGHT.P, IHF.RIGHT.M and IHF.LEFT.P, IHF.LEFT.M).

6.1.2.1 8-Ω Stereo Hands-Free Output Characteristics

Figure 6-4 shows the 8-Ω stereo hands-free amplifier. Table 6-2 lists the output characteristics of the 8-Ω stereo hands-free amplifier.

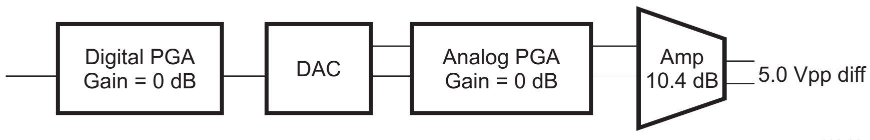


Figure 6-4. 8-Ω Stereo Hands-Free Amplifiers

Table 6-2. 8-Ω Stereo Hands-Free Output Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
VBAT voltage		3.0	3.6	4.6	V
Load impedance		6	8		Ω

Table 6-2. 8-Ω Stereo Hands-Free Output Characteristics (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain range(1)	Audio path	–75.6		34.4	dB
	Voice path	–49.6		34.4	
Absolute gain error		–1		1	dB
Maximum output power (load impedance = 8 Ω)	VBAT > 3.6 V		400		mW
	VBAT > 4.0 V		700		
Peak-to-peak differential output voltage	VBAT > 3.6 V (0 dBFs)		5.0		V_{PP}
	VBAT > 4.0 V (2 dBFs)		6.25		
Total harmonic distortion (load impedance = 8 Ω, gain setting = 0 dB) (VBAT > 3.6 V)	At 0 dBFs		–60	–40	dBFs
	At –10 dBFs			–60	
	At –20 dBFs			–45	
	At –60 dBFs			–20	
Total harmonic distortion (load impedance = 8 Ω, (VBAT > 4.2 V)	2 dBFs		–60	–40	dB
Idle channel noise (20 Hz to 20 kHz)	0 dB gain		–88		dBFs
PSRR (input signal 1 kHz sine, 300 mVPP GSM ripple at 217 Hz with 10-µs rise/fall times, at 12.5% duty cycle)	From VBAT	75	80		dB
Efficiency	Power on load = 400 mW Load impedance = 8 Ω	70%			
Power dissipation	Power on load = 400 mW Load impedance = 8 Ω			175	mW
Idle current consumption on VBAT	Without input signal		6		mA
Clock frequency for the ramp generation		384		426.6	kHz
I_{DDQ} current	At 25°C		0.6		µA

(1) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps)
Voice digital filter = –36 to 12 dB (1-dB steps)
ARXPGA (volume control) = –24 to 12 dB (2-dB steps)
Output driver = 10.4 dB

6.1.2.1.1 Short-Circuit Protection

There is short-circuit protection for hands-free amplifiers to limit power dissipation to 1.2 W. The short-circuit protection can be disabled by register. If a short circuit is detected, the short-circuit detection block switches off the hands-free speaker output stages. A software restart is required to restart the class-D amplifier.

6.1.2.2 External Components and Application Schematic

Figure 6-5 is a simplified schematic of the 8-Ω stereo hands-free.

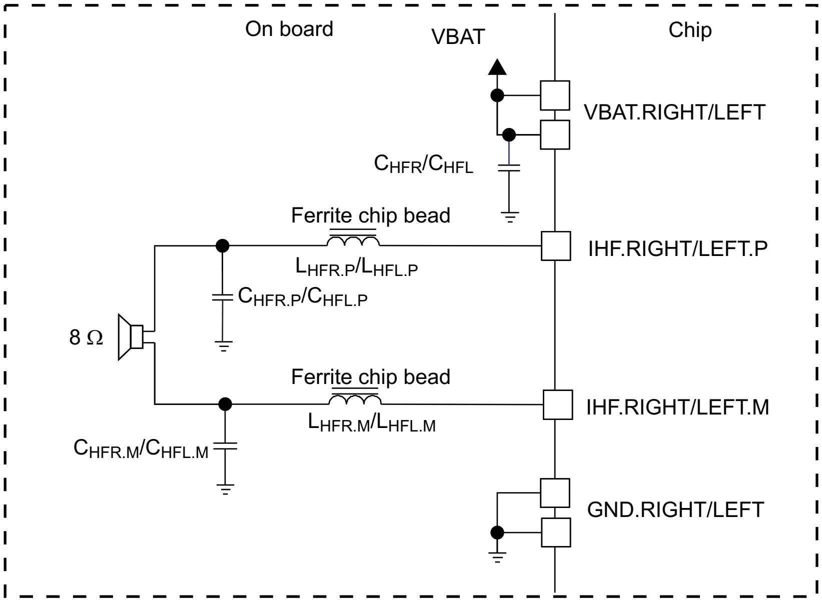


Figure 6-5. 8-Ω Stereo Hands-Free

NOTE

For the component values, see Table 15-1.

For ferrite bead, choose one with high impedance at high frequencies, but with very low impedance at low frequencies. For example, MPZ1608S221A (recommended), N2012ZPS121, or MDP BKP1608HS271.

6.1.3 *Headset*

The analog signal from the audio and/or voice interface is fed to two single-ended headset amplifiers.

There are two configurations:

- Stereo single-ended mode: Left and right headset amplifiers with different gains (–6, 0, 6 dB) provide the stereo signal on the HSOL and HSOR terminals. A pseudo-ground is provided on the VMID terminal to eliminate external capacitors.
- Stereo single-ended mode ac-coupled: Left and right headset amplifiers with different gains (–6, 0, 6 dB) provide the stereo signal on the HSOL and HSOR terminals. The external capacitor is required to eliminate the dc component of the signal.

6.1.3.1 Headset Output Characteristics

Figure 6-6 shows the headset amplifier. Table 6-3 lists the output characteristics of the headset amplifier.

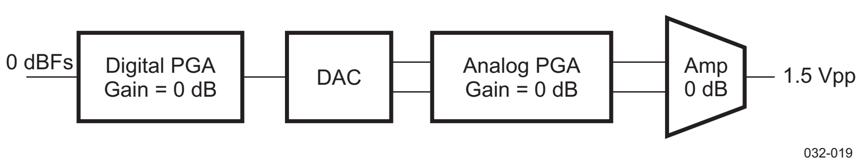


Figure 6-6. Headset Amplifier

Table 6-3. Headset Output Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Load impedance		14	16		Ω

Table 6-3. Headset Output Characteristics (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
		100	100		pF
Gain range (1)	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error		–1		1	dB
Maximum output power	At 0.53 Vrms differential output voltage Load impedance = 16 Ω		17.56		mW
Peak-to-peak output voltage (0 dBFs)	Default gain (2)		1.5		V_{PP}
Single-Ended Mode ac-Coupled					
Total harmonic distortion Default gain (2) Load = 16 Ω	At 0 dBFs		–80	–75	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–65	
	At –60 dBFs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain (3) Load = 16 Ω		–90	–85	dB
SNR (A-weighted over 20-kHz bandwidth)	At 0 dBFs	82	86		dB
Output PSRR (for all gains)	20 Hz to 4 kHz		90		dB
	20 Hz to 20 kHz		70		
Crosstalk between right and left channels			–60		dB
Single-Ended Mode (Pseudo-Ground Provided on HSOVMID)					
Total harmonic distortion Default gain (3) Load = 16 Ω	At 0 dBFs		–75	–70	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–65	
	At –60 dBFs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain (3) Load = 16 Ω		–90	–85	dB
Output PSRR (for all gains)	20 Hz to 4 kHz		85		dB
	20 Hz to 20 kHz		65		

(1) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps)
Voice digital filter = –36 to 12 dB (1-dB steps)
ARXPGA (volume control) = –24 to 12 dB (2-dB steps)
Output driver = –6, 0, 6 dB
(2) The default gain setting assumes the ARXPGA has 0 dB gain setting (volume control) and output driver at 0 dB gain setting.
(3) The default gain setting assumes the ARXPGA has 0 dB gain setting (volume control) and output driver at 0 dB gain setting.

6.1.3.2 External Components and Application Schematic

Figure 6-7 is a schematic of a headset 4-wire stereo jack without an external FET. Table 6-4 lists the output characteristics of this configuration.

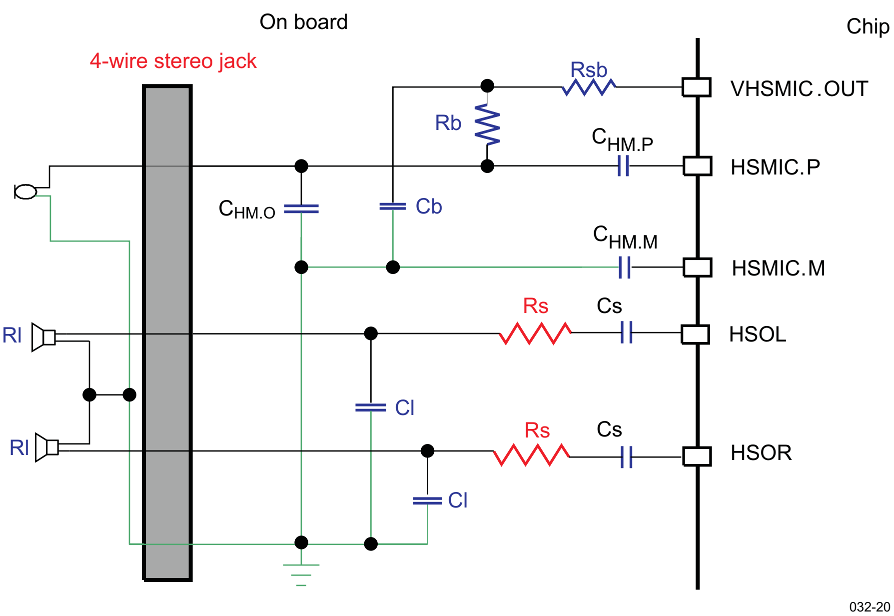


Figure 6-7. Headset 4-Wire Stereo Jack Without an External FET

Table 6-4. Output Characteristics of a Headset 4-Wire Stereo Jack Without an External FET

Parameter	Test Conditions		Min	Typ	Max	Unit
Rsb	Cb < 200 pF		0			Ω
	Cb = 100 nF		300			
	Cb = 1 µF		500			
Rb + Rsb			2.2		2.7	kΩ
Cs The input capacitors and output resistors form a high-pass filter (HPF) with the corner frequency = $1/(2\pi R_{out}/Cs)$			22	47		µF
	R_L	**C_L**				
Rs required to ensure	16 to 32 Ω	<100 pF	0			Ω
HS amplifier stability	16 to 32 Ω	1 nF	4			
	16 Ω	2 nF	8			
	24 Ω		12			
	32 Ω		18			
	16 Ω	3 nF	12			
	24 Ω		20			
	32 Ω		24			
	16 Ω	4 nF	16			
	24 Ω		24			
	32 Ω		32			
	16 Ω	5 nF	20			
	24 Ω		28			
	32 Ω		36			

NOTE

For other component values, see Table 15-1.

Table 6-5 is a schematic of a headset 4-wire stereo jack with an external FET. Table 6-5 lists the output characteristics of this configuration.

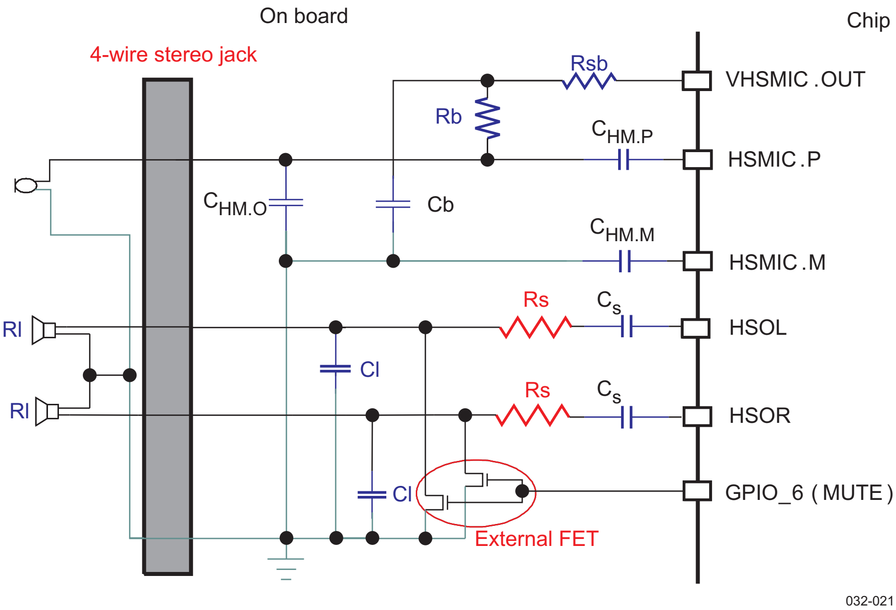


Figure 6-8. Headset 4-Wire Stereo Jack With an External FET

Table 6-5. Output Characteristics of a Headset 4-Wire Stereo Jack With an External FET

Parameter	Test Conditions		Min	Typ	Max	Unit
Rsb	Cb < 200 pF		0			Ω
	Cb = 100 nF		300			
	Cb = 1 μF		500			
Rb + Rsb			2.2		2.7	kΩ
Cs The input capacitors and output resistors form a HPF with the corner frequency = $1/(2\pi R_{out}/Cs)$			22	47		μF
Rs required to ensure HS amplifier stability and no distortion caused by the parasitic diode of the external FET	**R_L**	**C_L**				
	16 Ω	<2 nF	10			Ω
	24 Ω		15			
	32 Ω		20			
	16 Ω	3 nF	12			
	24 Ω		20			
	32 Ω		24			
	16 Ω	4 nF	16			
	24 Ω		24			
	32 Ω		32			
	16 Ω	5 nF	20			
	24 Ω		28			
	32 Ω		36			

NOTE

For other component values, see Table 15-1.

Figure 6-9 is a schematic of a headset 5-wire stereo jack. Table 6-6 lists the output characteristics of this configuration.

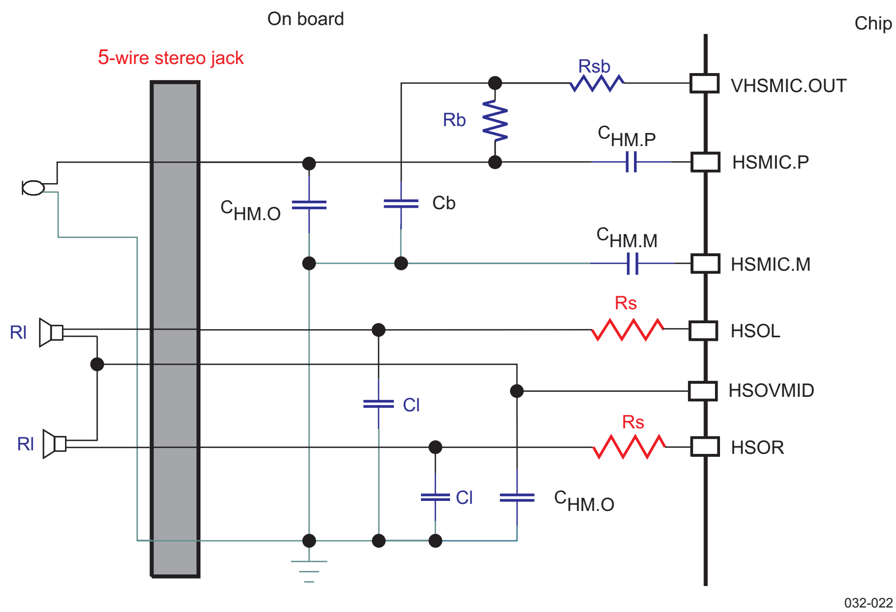


Figure 6-9. Headset 5-Wire Stereo Jack

Table 6-6. Output Characteristics of a Headset 5-Wire Stereo Jack

Parameter	Test Conditions		Min	Typ	Max	Unit
Rsb	Cb < 200 pF		0			Ω
	Cb = 100 nF		300			
	Cb = 1 μF		500			
Rb + Rsb			2.2		2.7	kΩ
	R_L	C_L				
Rs required to ensure HS amplifier stability	16 to 32 Ω	<100 pF	0			Ω
	16 to 32 Ω	1 nF	4			
	16 Ω	2 nF	8			
	24 Ω		12			
	32 Ω		18			
	16 Ω	3 nF	12			
	24 Ω		20			
	32 Ω		24			
	16 Ω	4 nF	16			
	24 Ω		24			
	32 Ω		32			
	16 Ω	5 nF	20			
	24 Ω		28			
	32 Ω		36			

NOTE

For other component values, see Table 15-1.

Figure 6-10 is a schematic of a headset 4-wire stereo jack optimized.

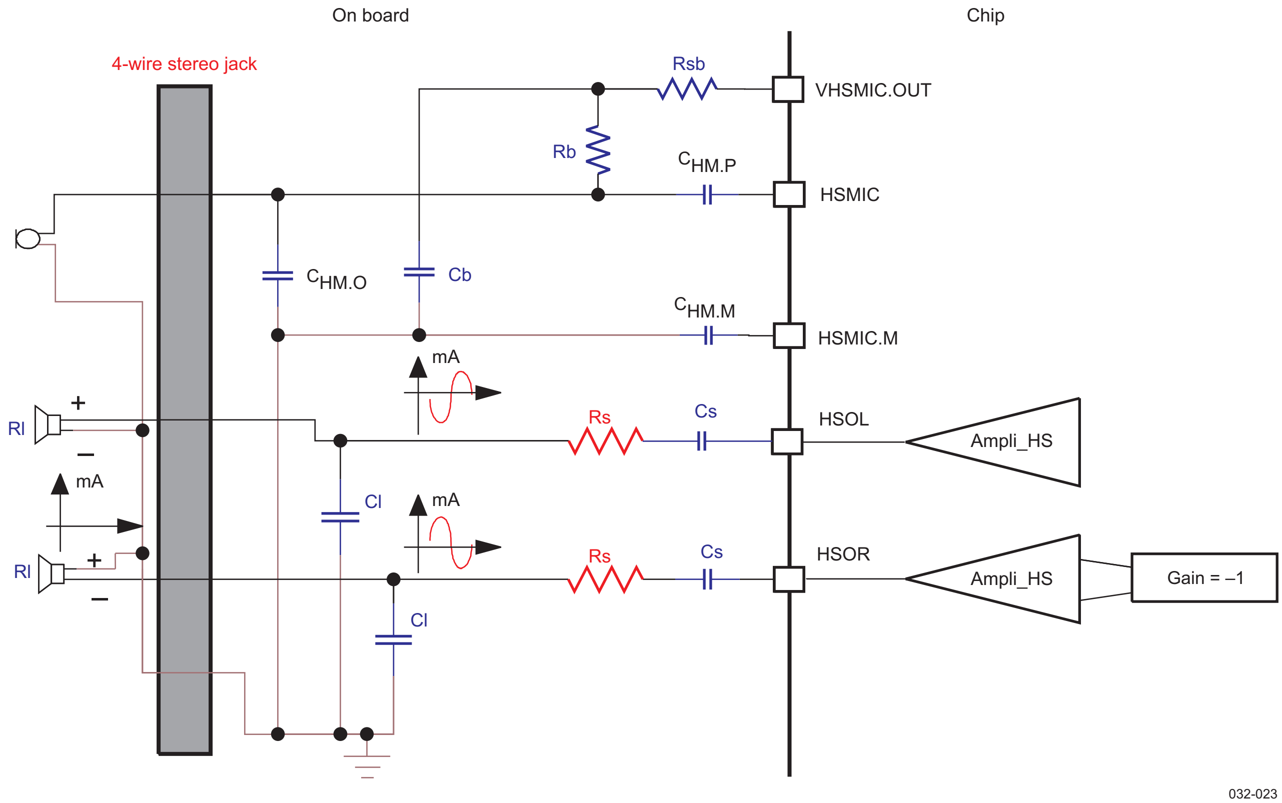


Figure 6-10. Headset 4-Wire Stereo Jack Optimized

NOTE

For other component values, see Table 15-1.

6.1.4 Headset Pop-Noise Attenuation

Pop noise occurs when the audio output amplifier is switched on. Although the speaker is ac-coupled through an external capacitor, the sharp rise time given by the activation of the amplifier causes a large spike to propagate to the speakers. Pop attenuation is achieved through a precharge and discharge of the external coupling capacitor.

The antipop system using an internal current generator controlling the ramp of charge or discharge is implemented for the headset output. The pop-noise effect can be dramatically reduced by an external FET controlled by a 1.8-V output signal (MUTE pin).

Figure 6-11 is a diagram of headset pop noise. Table 6-7 lists the characteristics of headset pop noise.

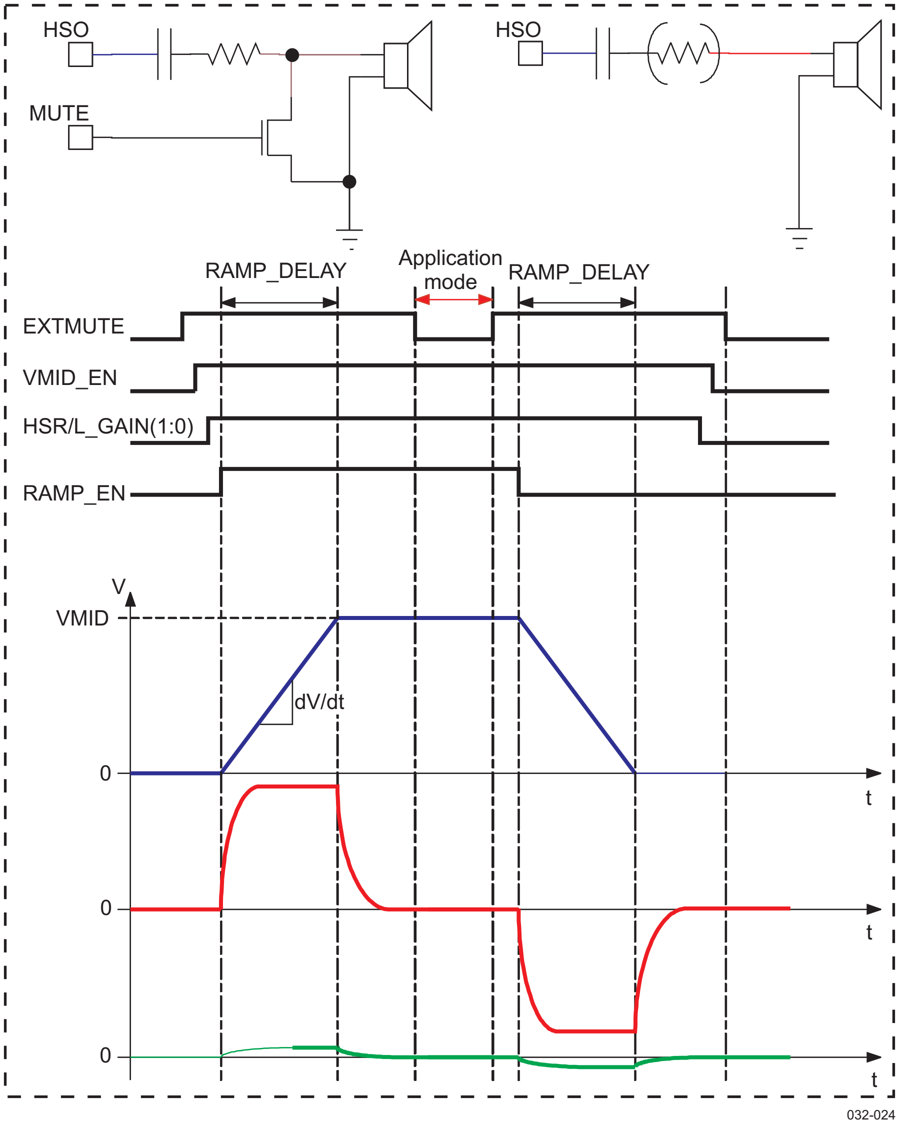


Figure 6-11. Headset Pop-Noise Cancellation Diagram

Table 6-7. Headset Pop-Noise Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
dv/dt	Ramp of charge or discharge			170	V/s
Pop-noise (A-weighted)	ac-coupling capacitor = 47 μF Serial resistor = 33 Ω External FET: Rdson = 0.12 Ω			1	mV

6.1.5 Predriver for External Class-D Amplifier

Two predriver amplifiers provide a stereo signal on the PreD.LEFT and PreD.RIGHT terminals to drive an external class-D amplifier. These terminals are available if a stereo, single-ended, ac-coupled headset is used.

6.1.5.1 Predriver Output Characteristics

Table 6-8 lists the output characteristics of the predriver.

Table 6-8. Predriver Output Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Load impedance		10			kΩ
		50			pF
Gain range (1)	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error		–1		1	dB
Peak-to-peak output voltage (0 dBFs)	Default gain (2)		1.5		V_{PP}
Total harmonic distortion Default gain (2) Load > 10 kΩ // 50 pF	At 0 dBFs		–80	–75	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–65	
	At –60 dBFs		–30	–25	
Idle channel noise (20 Hz to 20 kHz, A-weighted)	Default gain (3) Load = 10 Ω		–90	–85	dB
SNR (A-weighted over 20-kHz bandwidth) Default gain (3)	At 0 dBFs	83	88		dB
	At –60 dBFS		30		
Output PSRR (for all gains)	20 Hz to 4 kHz		90		dB
	20 Hz to 20 kHz		70		

(1) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps)
Voice digital filter = –36 to 12 dB (1-dB steps)
ARXPGA (volume control) = –24 to 12 dB (2-dB steps)
Output driver = –6, 0, 6 dB
(2) The default gain setting assumes the ARXPGA has a 0 dB gain setting (volume control) and output driver has a 0 dB gain setting.
(3) The default gain setting assumes the ARXPGA has a 0 dB gain setting (volume control) and output driver has a 0 dB gain setting.

6.1.5.2 External Components and Application Schematic

Figure 6-12 is a simplified schematic of the external class-D predriver.

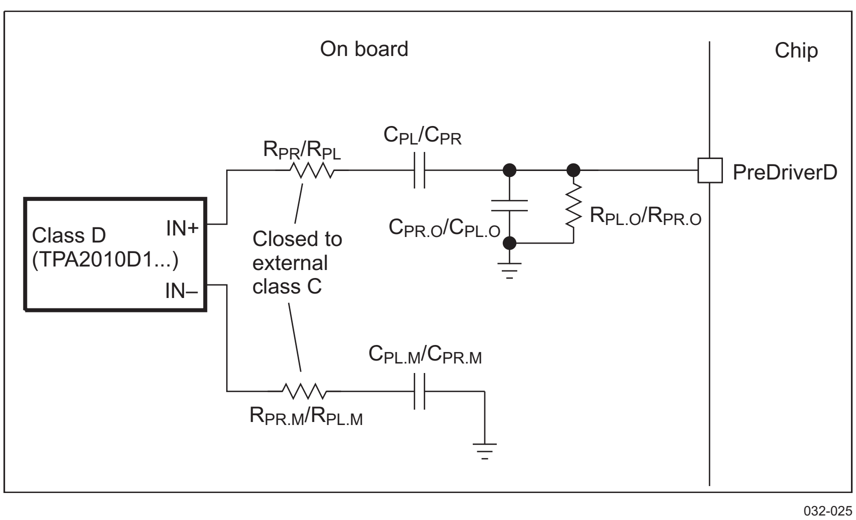


Figure 6-12. Predriver for External Class D

In Figure 6-12, input resistor (R_{PR} or R_{PL}) sets the gain of the external class D. For TPS2010D1, the gain is defined according to the following equation:

Gain (V/V) = $2*150*10^3/(R_{PR}$ or $R_{PL})$

R_{PR} or R_{PL} > 15 kΩ

NOTE

For other component values, see Table 15-1.

6.1.6 *Vibrator H-Bridge*

A digital signal from the pulse width modulated generator is fed to the vibrator H-bridge driver. The vibrator H-bridge is a differential driver that drives vibrator motors. The differential output allows dual rotation directions.

6.1.6.1 Vibrator H-Bridge Output Characteristics

Table 6-9 lists the output characteristics of the vibrator H-bridge.

Table 6-9. Vibrator H-Bridge Output Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
VBAT voltage		2.8	3.6	4.8	V
Differential output swing (16-Ω load)	VBAT = 2.8 V	3.6			V_{PP}
	VBAT = 3.5 V	4.3			
Output resistance (summed for both sides)				8	Ω
Load capacitance				100	pF
Load resistance		8	16	60	Ω
Load inductance			30	300	µH
Total harmonic distortion				10%	
Operating frequency		20		10k	Hz

6.1.6.2 External Components and Application Schematic

Figure 6-13 is a simplified schematic of the vibrator H-bridge.

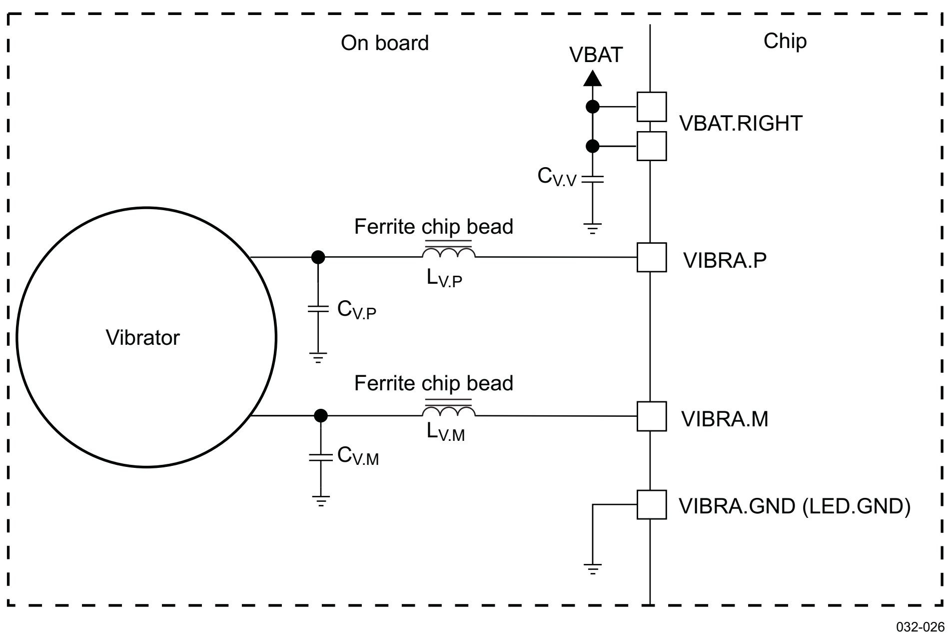


Figure 6-13. Vibrator H-Bridge

NOTE

For other component values, see Table 15-1.

Example of ferrite: BLM 18BD221SN1.

6.1.7 *Carkit Output*

The USB-CEA carkit uses the DP/DM pad to output audio signals (see the *CEA-936A: Mini-USB Analog Carkit Interface Specification*).

The MCPC carkit uses the RXAF analog pad to output audio signals.

Figure 6-14 shows the carkit output downlink full path characteristics for audio and USB.

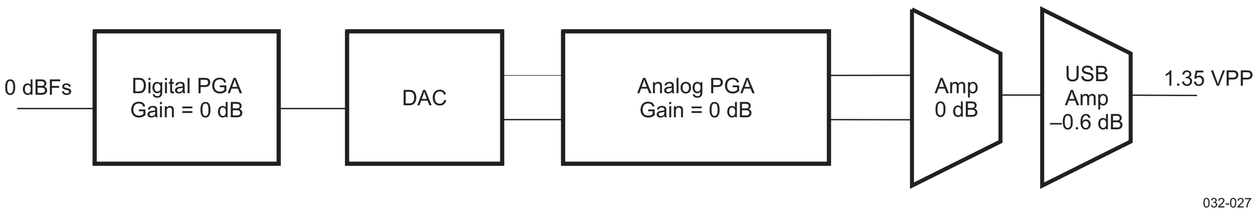


Figure 6-14. Carkit Output Downlink Path Characteristics

Table 6-10 lists the electrical characteristics of the MCPC and USB-CEA carkit audio.

Table 6-10. MCPC and USB-CEA Carkit Audio Downlink Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Output load	USB-CEA (DP/DM)	20			kΩ
	MCPC (RXAF)	5			
Gain range(1)	Audio path	–92		30	dB
	Voice path	–66		30	
Absolute gain error	At 1 kHz	–1		1	dB
Peak-to-peak differential output voltage (0 dBFs)	Gain = 0 dB		1.5		V_{PP}
Total harmonic distortion	At 0 dBFs		–80	–75	dB
	At –6 dBFs		–74	–69	
	At –20 dBFs		–70	–65	
	At –60 dBFs		–30	–25	
THD+N (20 Hz to 20 kHz, A-weighted)	At 0 dBFs		60		dB
Idle channel noise (20 Hz to 20 kHz, A-weighted), default gain setting(2)	USB-CEA		–77		dBFs
	MCPC		–80	–77	
Output PSRR	20 Hz to 20 kHz		60		dB
Supply voltage (VINTANA1)			1.5		V
Common mode output voltage for USB-CEA		1.3	1.35	1.4	V
Isolation between D+/D– during audio mode (20 Hz to 20 kHz)		60			dB
Crosstalk between right and left channels	USB-CEA stereo		–90		dB
Crosstalk RX/TX (1 V_{PP} output)	USB-CEA mono/stereo			–60	dB
	MCPC			–65	
Signal noise ratio (20 Hz to 20 kHz, A-weighted)	At 0 dBFs		60		dB

(1) Audio digital filter = –62 to 0 dB (1-dB steps) and 0 to 12 dB (6-dB steps);
Voice digital filter = –36 to 12 dB (1-dB steps);
ARXPGA (volume control) = –24 to 12 dB (2-dB steps);
Output driver (USB-CEA and MCPC) = –1 dB

(2) The default gain setting assumes the ARXPGA has 0-dB gain setting (volume control) and output driver at 0.6-dB gain setting.

Table 6-10. MCPC and USB-CEA Carkit Audio Downlink Electrical Characteristics (continued)

Parameter	Conditions	Min	Typ	Max	Unit
Phone speaker amplifier output impedance at 1 kHz	USB-CEA (DP/DM)			200	Ω
	MCPC (RXAF)			200	

6.1.8 Digital Audio Filter Module

Figure 6-15 shows the digital audio filter downlink full path characteristics of the audio interface.

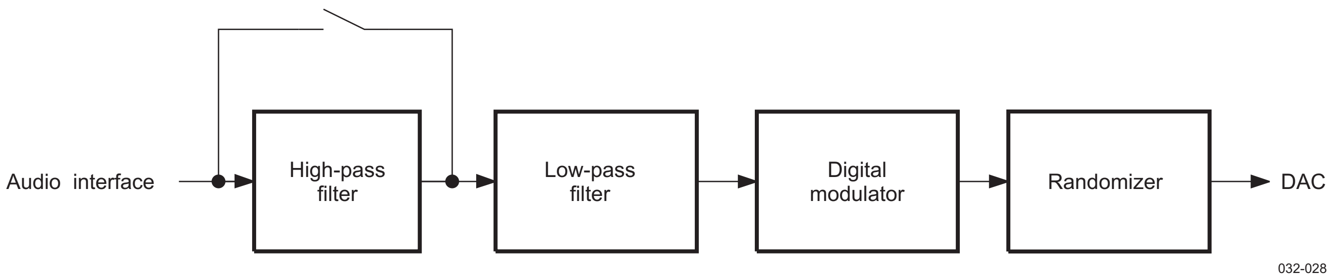


Figure 6-15. Digital Audio Filter Downlink Path Characteristics

The HPF can be bypassed.

Table 6-11 lists the audio filter frequency responses relative to reference gain at 1 kHz.

Table 6-11. Digital Audio Filter RX Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Passband			0.42		F_S
Passband ripple	0 to 0.42F_S (1)	–0.25	0.1	0.25	dB
Stopband			0.6		F_S
Stopband attenuation	F = 0.6F_S (1) to 0.8F_S (1)	60	75		dB
Group delay			15.8/F_S (1)		μs
Linear phase		–1.4		1.4	°

(1) F_S is the sampling frequency (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz).

6.1.9 Digital Voice Filter Module

Figure 6-16 shows the digital voice filter downlink full path characteristics of the voice interface.

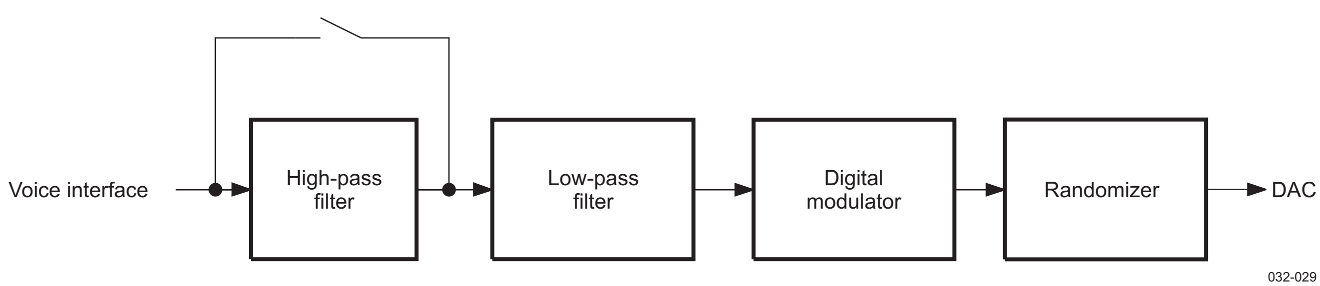


Figure 6-16. Digital Voice Filter Downlink Path Characteristics

The global HPF or only the third-order HPF can be bypassed (when the third-order HPF is skipped, the first-order HPF remains active).

6.1.9.1 Voice Downlink Filter (Sampling Frequency at 8 kHz)

Figure 6-17 shows the voice downlink frequency response with F_S = 8 kHz. Table 6-12 lists the voice filter frequency responses relative to the reference gain at 1 kHz with F_S = 8 kHz.

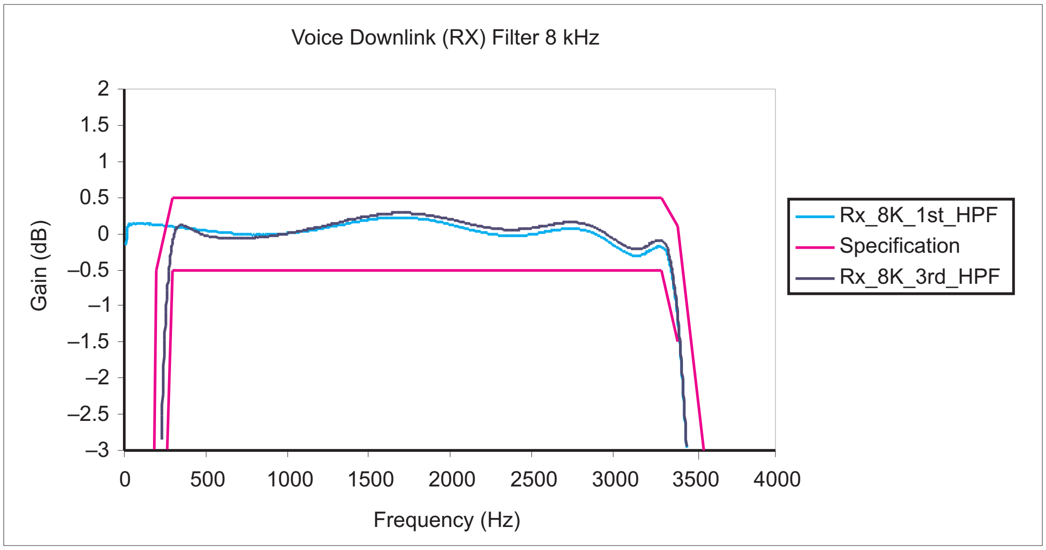


Figure 6-17. Voice Downlink Frequency Response With F_S = 8 kHz

Table 6-12. Digital Voice Filter RX Electrical Characteristics With F_S = 8 kHz

Parameter	Test Conditions	Min	Typ	Max	Unit
Frequency response relative to reference gain at 1 kHz (first-order HPF)	100 Hz			–20	dB
	200 Hz	–8		–0.5	
	300 to 3300 Hz	–0.5	0	0.5	
	3400 Hz	–1.5	0	0.1	
	4000 Hz			–17	
	4600 Hz			–40	
	> 6000 Hz			–45	
Pole when third-order HPF is disabled (first-order HPF)			2.5		Hz
Group delay			0.5		ms

6.1.9.2 Voice Downlink Filter (Sampling Frequency at 16 kHz)

Figure 6-18 shows the voice downlink frequency response with F_S = 16 kHz. Table 6-13 lists the voice filter frequency responses relative to the reference gain at 1 kHz with F_S = 16 kHz.

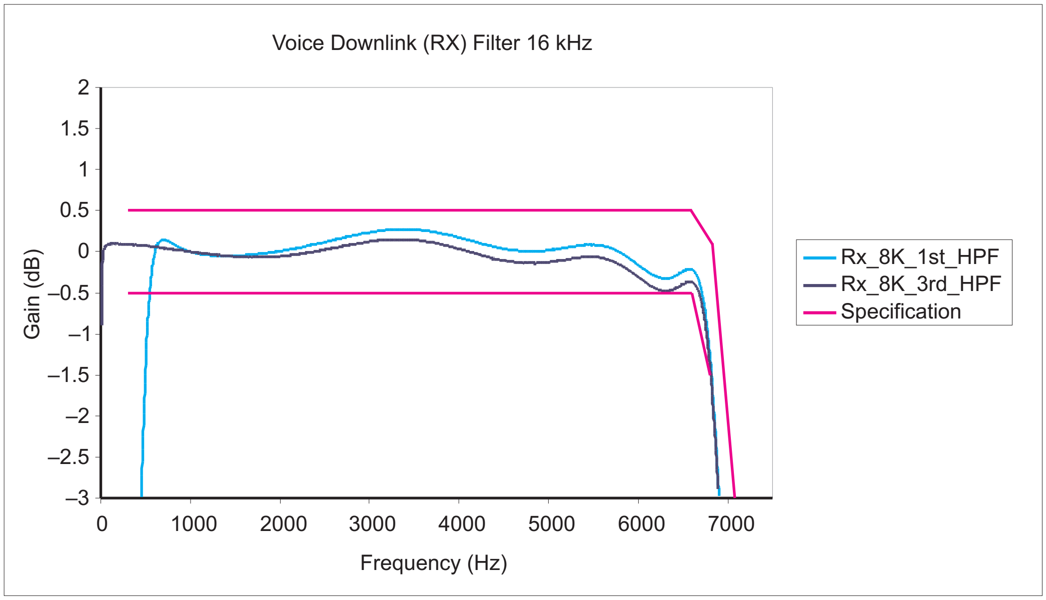


Figure 6-18. Voice Downlink Frequency Response With F_S = 16 kHz

Table 6-13. Digital Voice Filter RX Electrical Characteristics With F_S = 16 kHz

Parameter	Test Conditions	Min	Typ	Max	Unit
Frequency response relative to reference gain at 1 kHz (first-order HPF)	300 to 6600 Hz	–0.5	0	0.5	dB
	6800 Hz	–1.5	0	0.1	
	8000 Hz			–17	
	9200 Hz			–40	
	> 12000 Hz			–45	
Pole when third-order HPF is disabled (first-order HPF)			5		Hz

6.1.10 Boost Stage

The boost effect adds emphasis to low frequencies. It compensates for an HPF created by the capacitance resistor (CR) filter of the headset (in ac-coupling configuration).

There are four modes. Three effects are available, with slightly different frequency responses, and the fourth setting disables the boost effect:

- Boost effect 1
- Boost effect 2
- Boost effect 3
- Flat equalization: The boost effect is in bypass mode.

Table 6-14 and Table 6-15 list typical values according to frequency response versus input frequency and F_S frequency.

Table 6-14. Boost Electrical Characteristics Versus F_S Frequency ($F_S \leq 22.05$ kHz)

Frequency (Hz)	F_S = 8 kHz			F_S = 11.025 kHz			F_S = 12 kHz			F_S = 16 kHz			F_S = 22.05 kHz			Unit
	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	
10	4.51	5.13	5.62	5.10	5.51	5.80	5.22	5.58	5.83	5.54	5.77	5.92	5.76	5.89	5.97	dB
12	4.08	4.83	5.46	4.80	5.32	5.71	4.95	5.41	5.76	5.36	5.66	5.87	5.65	5.83	5.94	
15.2	3.43	4.32	5.18	4.28	4.97	5.54	4.47	5.11	5.61	5.03	5.47	5.79	5.45	5.71	5.90	
18.2	2.91	3.86	4.89	3.82	4.63	5.36	4.04	4.80	5.45	4.71	5.26	5.69	5.24	5.59	5.84	
20.5	2.56	3.53	4.65	3.49	4.37	5.21	3.72	4.56	5.32	4.45	5.09	5.60	5.06	5.49	5.79	
29.4	1.62	2.49	3.78	2.45	3.42	4.57	2.68	3.74	4.73	3.51	4.39	5.24	4.35	5.02	5.59	
39.7	1.05	1.71	2.93	1.67	2.55	3.84	1.88	2.80	4.06	2.66	3.63	4.72	3.67	4.45	5.27	
50.4	0.71	1.20	2.26	1.17	1.91	3.17	1.33	2.13	3.41	2.01	2.95	4.19	2.89	3.85	4.88	
60.3	0.51	0.92	1.79	0.89	1.49	2.65	1.00	1.68	2.89	1.57	2.43	3.72	2.39	3.35	4.52	
76.7	0.32	0.61	1.26	0.59	1.05	1.99	0.69	1.18	2.22	1.11	1.79	3.04	1.76	2.66	3.94	
97.5	0.20	0.39	0.87	0.38	0.70	1.43	0.44	0.79	1.62	0.75	1.27	2.36	1.24	2.00	3.28	
131.5	0.12	0.21	0.50	0.20	0.39	0.88	0.25	0.47	1.02	0.42	0.78	1.59	0.75	1.30	2.41	
157	0.08	0.15	0.36	0.15	0.28	0.65	0.17	0.33	0.75	0.31	0.57	1.22	0.55	0.99	1.93	
200	0.05	0.09	0.22	0.09	0.17	0.41	0.11	0.21	0.49	0.19	0.37	0.82	0.36	0.66	1.38	
240	0.03	0.06	0.15	0.06	0.12	0.29	0.07	0.14	0.35	0.14	0.26	0.60	0.25	0.48	1.04	
304	0.02	0.04	0.09	0.04	0.07	0.18	0.04	0.09	0.22	0.08	0.16	0.38	0.16	0.30	0.70	
463	0.00	0.01	0.03	0.01	0.03	0.07	0.02	0.04	0.09	0.03	0.07	0.17	0.07	0.13	0.32	
704	0.00	0.00	0.01	0.00	0.01	0.03	0.01	0.01	0.03	0.01	0.03	0.07	0.03	0.06	0.14	
1008	0.00	0.00	0.00	0.00	0.00	0.01	0.00	0.00	0.01	0.00	0.01	0.03	0.01	0.02	0.06	
1444	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.02	
2070	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.01	
3770	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	

Table 6-15. Boost Electrical Characteristics Versus F_S Frequency ($F_S \geq 24$ kHz)

Frequency (Hz)	F_S = 24 kHz			F_S = 32 kHz			F_S = 44.1 kHz			F_S = 48 kHz			F_S = 96 kHz			Unit
	1	2	3	1	2	3	1	2	3	1	2	3	1	2	3	
10	5.79	5.90	5.97	5.89	5.89	5.99	5.95	5.98	6.04	5.96	5.99	6.01	5.71	5.83	5.90	dB
12	5.70	5.85	5.95	5.84	5.84	5.98	5.92	5.97	6.03	5.94	5.98	6.00	5.54	5.68	5.81	
15.2	5.53	5.76	5.91	5.73	5.73	5.96	5.87	5.94	6.02	5.89	5.95	5.99	5.40	5.57	5.73	
18.2	5.35	5.65	5.87	5.62	5.62	5.93	5.80	5.90	6.00	5.83	5.93	5.98	5.28	5.48	5.68	
20.5	5.19	5.56	5.83	5.52	5.52	5.91	5.74	5.87	5.99	5.78	5.90	5.97	5.19	5.42	5.64	
29.4	4.55	5.18	5.64	5.10	5.07	5.79	5.51	5.75	5.94	5.57	5.79	5.92	4.87	5.18	5.48	
39.7	3.81	4.62	5.37	4.52	4.52	5.64	5.12	5.53	5.85	5.26	5.59	5.84	4.47	4.91	5.30	
50.4	3.14	4.06	5.02	3.94	3.95	5.43	4.69	5.27	5.72	4.88	5.37	5.73	4.08	4.63	5.11	
60.3	2.62	3.51	4.69	3.46	3.54	5.21	4.30	5.00	5.59	4.49	5.13	5.62	3.72	4.37	4.95	
76.7	1.97	2.90	4.15	2.76	2.76	4.78	3.68	4.52	5.34	3.91	4.70	5.40	3.18	3.92	4.67	
97.5	1.41	2.22	3.51	2.10	2.09	4.27	2.99	3.94	4.99	3.24	4.15	5.07	2.59	3.41	4.33	
131.5	0.88	1.49	2.65	1.40	1.40	3.49	2.15	3.10	4.35	2.38	3.35	4.51	1.86	2.69	3.75	
157	0.65	1.13	2.15	1.04	1.04	2.96	1.70	2.58	3.90	1.90	2.82	4.08	1.47	2.24	3.35	
200	0.41	0.76	1.55	0.70	0.70	2.28	1.19	1.93	3.23	1.35	2.15	3.44	1.03	1.68	2.77	
240	0.30	0.55	1.18	0.50	0.50	1.81	0.89	1.51	2.71	1.02	1.70	2.92	0.77	1.31	2.32	
304	0.18	0.35	0.80	0.33	0.32	1.27	0.58	1.04	2.05	0.68	1.19	2.24	0.51	0.90	1.75	
463	0.08	0.16	0.37	0.14	0.14	0.64	0.27	0.50	1.12	0.31	0.58	1.25	0.23	0.43	0.95	
704	0.03	0.06	0.16	0.06	0.06	0.29	0.12	0.23	0.56	0.14	0.27	0.62	0.10	0.20	0.46	
1008	0.01	0.03	0.07	0.03	0.02	0.14	0.06	0.11	0.30	0.06	0.13	0.31	0.05	0.10	0.23	
1444	0.00	0.01	0.03	0.01	0.01	0.06	0.03	0.05	0.16	0.03	0.06	0.15	0.02	0.05	0.11	
2070	0.00	0.00	0.01	0.00	0.00	0.02	0.01	0.02	0.09	0.01	0.03	0.07	0.01	0.02	0.05	
3770	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.04	0.00	0.00	0.01	0.00	0.00	0.01	

6.2 Audio/Voice Uplink (TX) Module

The voice uplink path includes two input amplification stages dedicated to ten analog input terminals:

- MIC_MAIN_P, MIC_MAIN_M (differential main handset input)
- MIC_SUB_P, MIC_SUB_M (differential sub handset input)
- HSMICP, HSMICM (differential headset input)
- AUXL (common terminal: single-ended auxiliary/FM radio left channel input)
- AUXR (common terminal: single-ended auxiliary/FM radio right channel input)
- CEA carkit and MCPC transmit audio (TXAF) microphone through DINP/DINM pins

For all cases, only two analog input amplifiers can be used, because two ADCs are available.

The voice uplink path also includes two pulse density modulated (PDM) interfaces for digital microphones. Two stereo digital microphone interfaces are available.

The left and right FM channels can be connected to any audio output stage (for example, earpiece, headset speakers, etc.) through a connection matrix.

6.2.1 Microphone Bias Module

Three bias generators provide an external voltage of 2.2 V to bias the analog microphones (MICBIAS1, MICBIAS2, and HSMICBIAS terminals). The typical output current is 1 mA for each analog bias microphone.

Two bias generators can provide an external voltage of 1.8 V to bias digital microphones (DIGMIC_0 and DIGMIC_1). The typical output current is 5 mA for each digital bias microphone.

NOTE

One bias generator can bias two digital microphones at the same time; in this case, the typical output current is 10 mA.

Figure 6-19 shows the multiplexing for the analog and digital microphones.

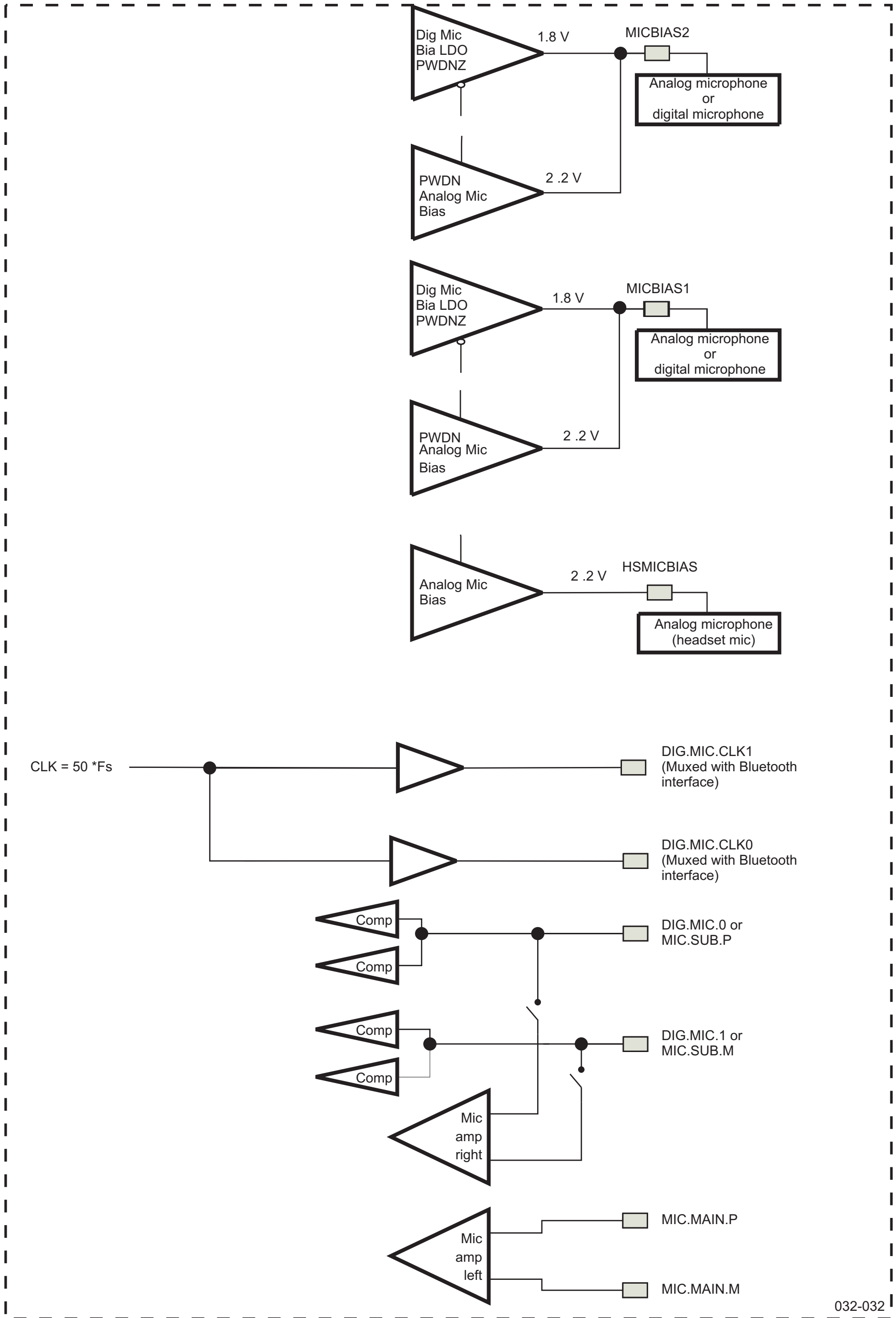


Figure 6-19. Analog and Digital Microphone Multiplexing

6.2.1.1 Analog Microphone Bias Module Characteristics

Table 6-16 lists the characteristics of the analog microphone bias module.

Table 6-16. Analog Microphone Bias Module Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Bias voltage		2.15	2.2	2.25	V
Load current				1	mA

Table 6-16. Analog Microphone Bias Module Characteristics (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Output noise	P-weighted 20 Hz to 6.6 kHz			1.8	μV_{RMS}
External capacitor		0		200	pF
Internal resistance		50	60	70	kΩ

NOTE

If the value of the external capacitor is greater than 200 pF, the analog microphone bias becomes unstable. To stabilize it, a serial resistor must be added.

Table 6-17 lists the characteristics of the analog microphone bias module with a bias resistor.

Table 6-17. Characteristics of Analog Microphone Bias Module With a Bias Resistor

Parameter	Test Conditions	Min	Typ	Max	Unit
R_{SB}	C_B < 200 pF	0			Ω
	C_B = 100 pF	300			
	C_B = 1 µF	500			
$R_B + R_{SB}$			2.2 to 2.7		kΩ

6.2.1.2 External Components and Application Schematic

Figure 6-20 and Figure 6-21 show the external components and application schematics for the analog microphone.

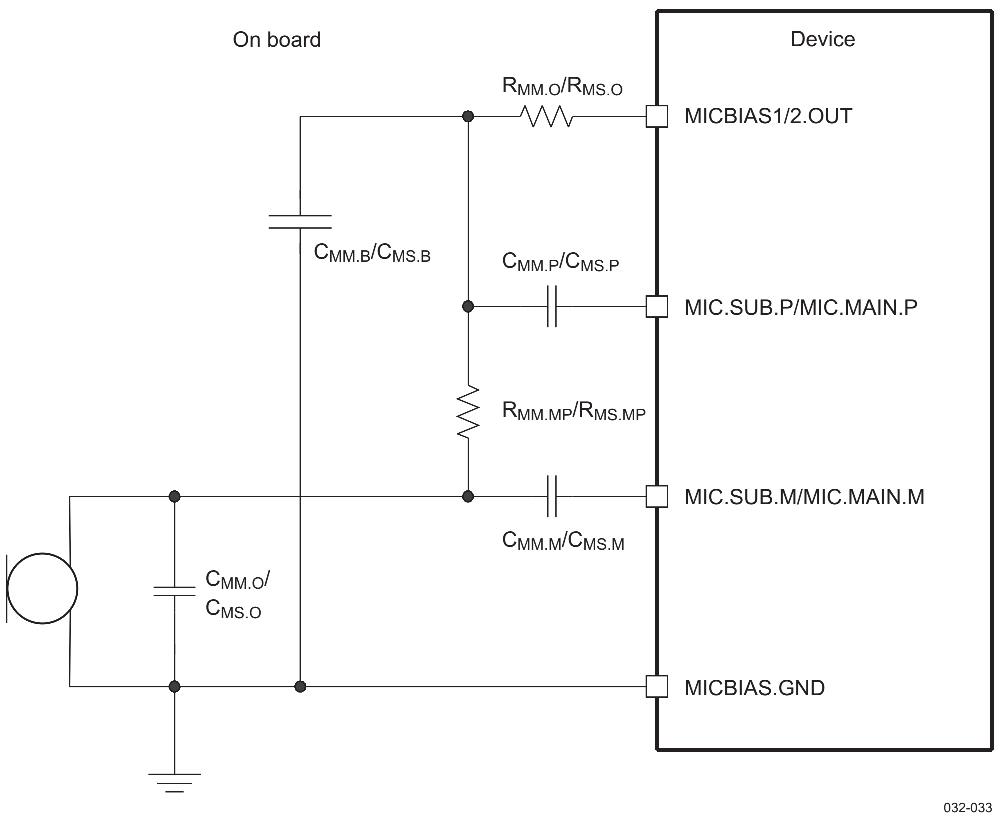


Figure 6-20. Analog Microphone Pseudodifferential

NOTE

For other component values, see Table 15-1.

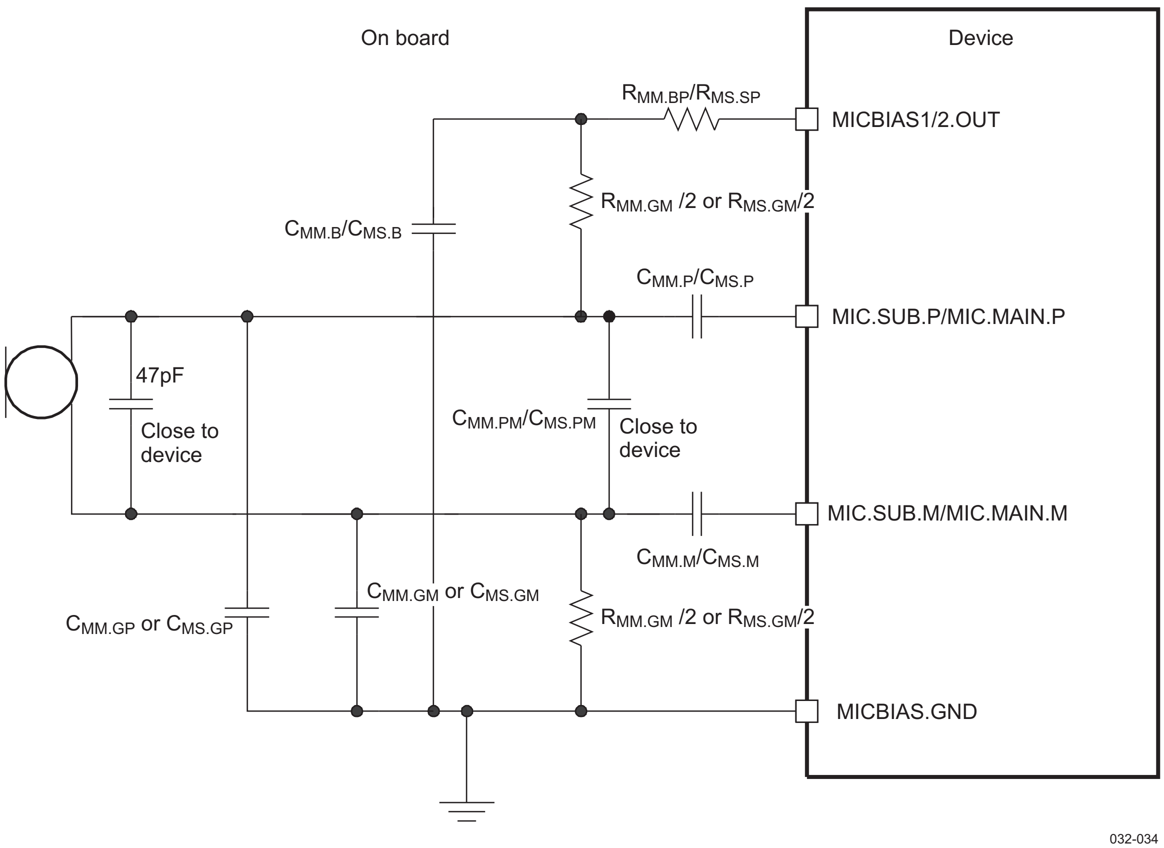


Figure 6-21. Analog Microphone Differential

NOTE

For other component values, see Table 15-1.

NOTE

To improve the rejection, it is highly recommended to ensure that MICBIAS_GND is as clean as possible. This ground must be shared with AGND of TPS65950 and must not share with AVSS4, which is the ground used by RX class-AB output stages.

In differential mode, adding a low-pass filter (made by R_{SB} and C_B) is highly recommended if coupling between RX output stages and the microphone is too high (and there is not enough attenuation by the echo cancellation algorithm). The coupling can come from:

- The internal TPS65950 coupling between MICBIAS.OUT voltage and RX output stages
- Coupling noise between MICBIAS.GND and AVSS4

In pseudodifferential mode, the dynamic resistance of the microphone improves the rejection versus MICBIAS.OUT:

$$PSRR = 20*\log((R_B + R_{Dyn_mic})/R_B)$$

6.2.1.3 Digital Microphone Bias Module Characteristics

Figure 6-22 is a block diagram of the digital microphone bias module.

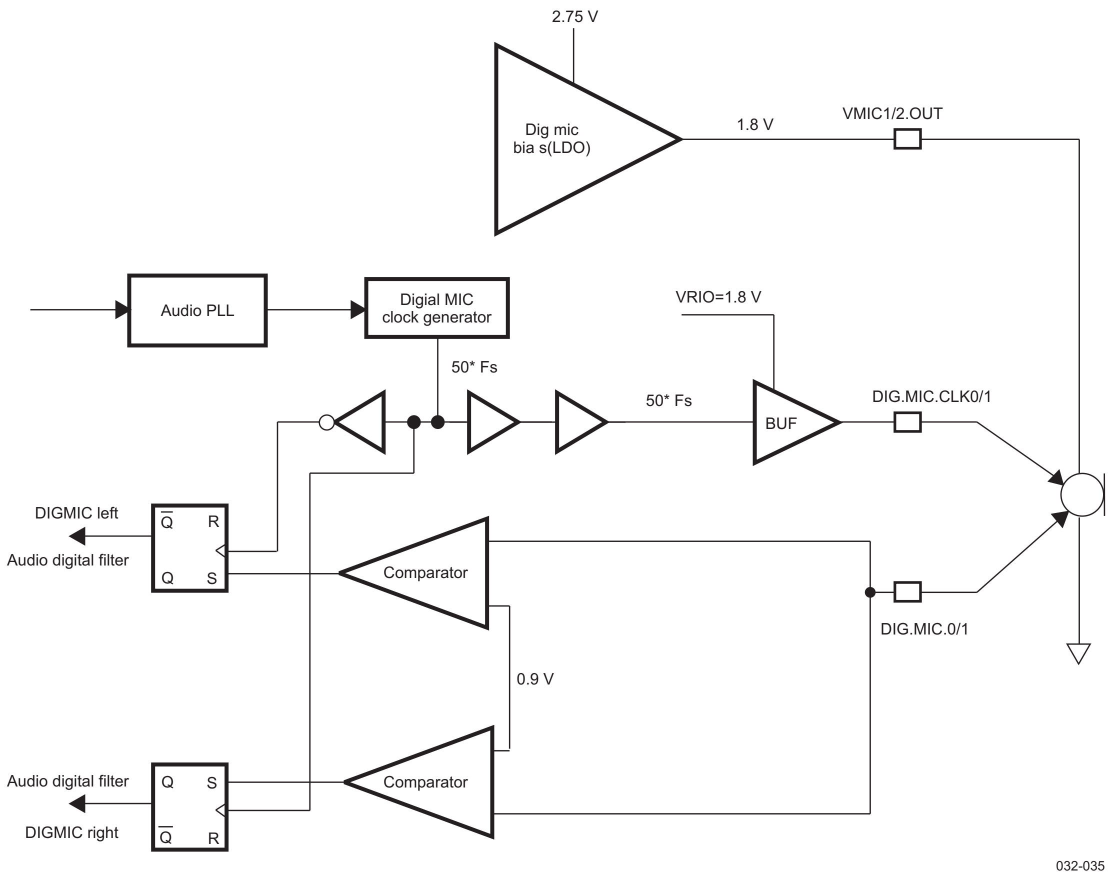


Figure 6-22. Digital Microphone Bias Module Block Diagram

Table 6-18 and Table 6-19 list the characteristics of the digital microphone bias module.

Table 6-18. Digital Microphone Bias Module Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Bias voltage			1.8		V
Load current				10	mA
PSRR (from VBAT)	20 Hz to 6.6 kHz	60			dB
External capacitor		0.3	1	3.3	µF
ESR for capacitor	At 100 kHz	0.02		0.6	Ω

Table 6-19. Digital Microphone Bias Module Characteristics (2)

Parameter	Test Conditions	Min	Typ	Max	Unit
Comparator high threshold			0.5*VDD_IO	0.7*VDD_IO	
Comparator low threshold		0.3*VDD_IO	0.5*VDD_IO		
Startup time				2	µs
DIG.MIC.0 (t_{HOLD}) from DIG.MIC.CLK0 edge		4			ns
DIG.MIC.1 (t_{HOLD}) from DIG.MIC.CLK1 edge		4			ns

Figure 6-23 is a timing diagram of the digital microphone bias module.

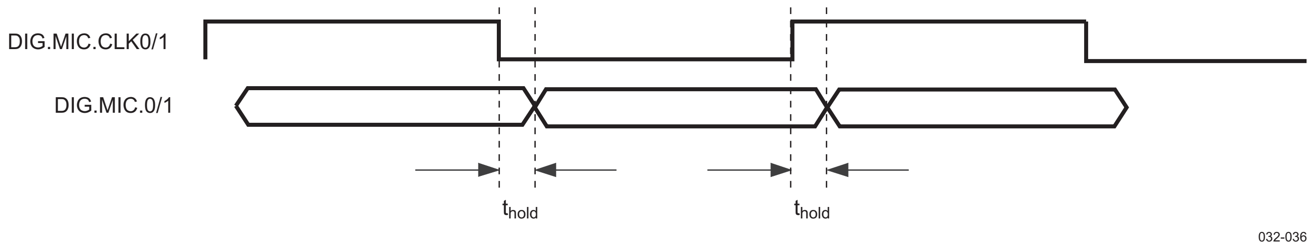


Figure 6-23. Digital Microphone Bias Module Timing Diagram

6.2.1.4 Silicon Microphone Characteristics

Based on silicon micro-electrical-mechanical system (MEMS) technology, the new microphone achieves the same acoustic and electrical properties as conventional microphones, but is more rugged and exhibits higher heat resistance. These properties offer designers greater flexibility and new opportunities to integrate microphones.

The silicon microphone is the integration of mechanical elements and electronics on a common silicon substrate through microfabrication technology.

The complementary metal oxide semiconductor (CMOS) MEMS microphone is more like an analog IC than a classic electric condenser microphone (ECM). It is powered as an IC with a direct connection to the power supply. The on-chip isolation between the power input and the rest of the system adds power supply rejection (PSR) to the component, making the CMOS MEMS microphone inherently more immune to power supply noise than an ECM and eliminating the need for additional filtering circuitry to keep the power supply line clean.

Figure 6-24 is a schematic of the silicon microphone module.

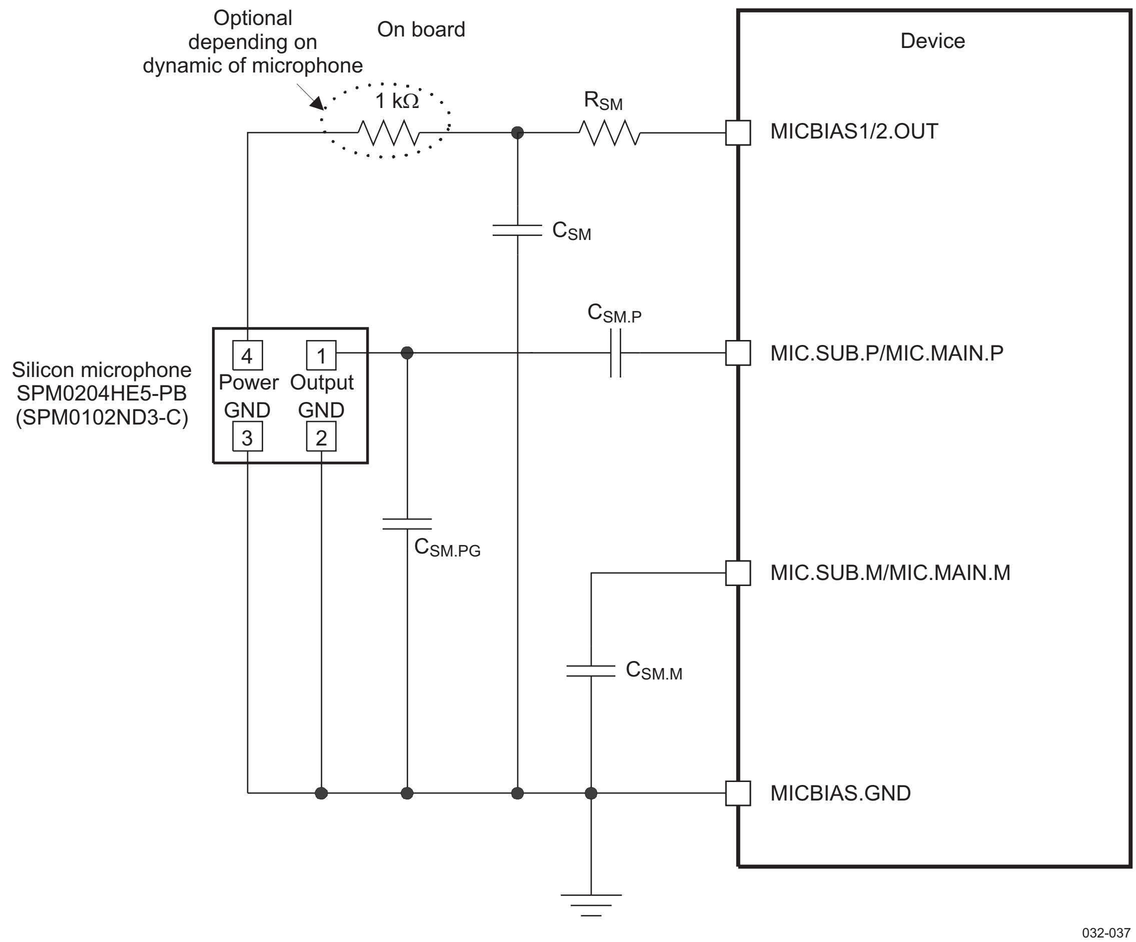


Figure 6-24. Silicon Microphone Module

Table 6-20 lists the characteristics of the silicon microphone module.

Table 6-20. Silicon Microphone Module Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Bias voltage			2.2		V
Load current				1	mA
Output noise	P-weighted 20 Hz to 6.6 kHz			1.8	μV_{RMS}

NOTE

For other component values, see Table 15-1.

6.2.2 Stereo Differential Input

The stereo differential inputs (the MIC_MAIN_P and MIC_MAIN_M, and the MIC_SUB_P and MIC_SUB_M terminals) can be amplified by the microphone amplification stages. The amplification stage outputs are connected to the two ADC inputs.

6.2.3 Headset Differential Input

The headset differential inputs (the HSMICP and HSMICM terminals) can be amplified by the microphone amplification stage. The amplification stage outputs are connected to the ADC input.

6.2.4 FM Radio/Auxiliary Stereo Input

The auxiliary inputs AUXL/FML and AUXR/FMR can be used as the left and right stereo inputs, respectively, of the FM radio. In that case (because both input amplifiers are busy), the other input terminals are discarded and set to a high-impedance state. Both microphone amplification stages amplify the FM radio stereo signal. Both amplification stage outputs are connected to the ADC input. The left and right channel inputs of the FM radio can also be output through an audio output stage (mono output stage in case of mono input FM radio, stereo output stage in case of stereo input FM radio).

6.2.4.1 External Components

Figure 6-25 shows the external components of the auxiliary stereo input.

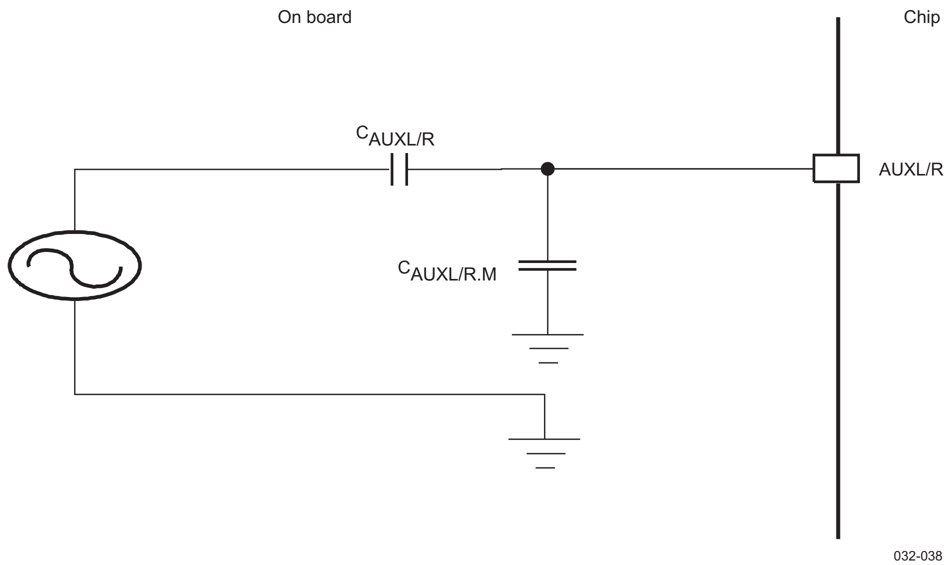


Figure 6-25. Audio Auxiliary Input

NOTE

For other component values, see Table 15-1.

6.2.5 PDM Interface for Digital Microphones

The PDM interface is used as digital microphone inputs; each microphone is directly connected to the TX filter decimator to extract the audio samples at the desired accuracy and sample rate. Each digital microphone is stereo (two paths). The digital microphone interface is DIG.MIC.CLK (clock input to the microphone) and DIG.MIC (PDM data output from the microphone). The appropriate frequency of DIG.MIC.CLK is generated by the audio PLL, and the ratio between DIG.MIC.CLK and the sample rate is 50 (see Figure 6-26). The PDM interface is available only when F_S = 48 kHz.

The data signal output is a 3-state output from the microphone. When a falling-edge DIG.MIC.CLK is detected, DIG.MIC is actively driven. When a rising DIG.MIC.CLK is detected, DIG.MIC is high impedance. The latter DIG.MIC.CLK half-cycle is reserved for stereo operation (the second microphone receives DIG.MIC.CLK inverted).

The Σ-Δ converter in the digital microphones produces PDM.

Digital microphone characteristics:

- PDM clock rate 2.4 MHz
- Fourth-order Σ-Δ converter in the microphone component

Figure 6-26 is an example of PDM interface circuitry.

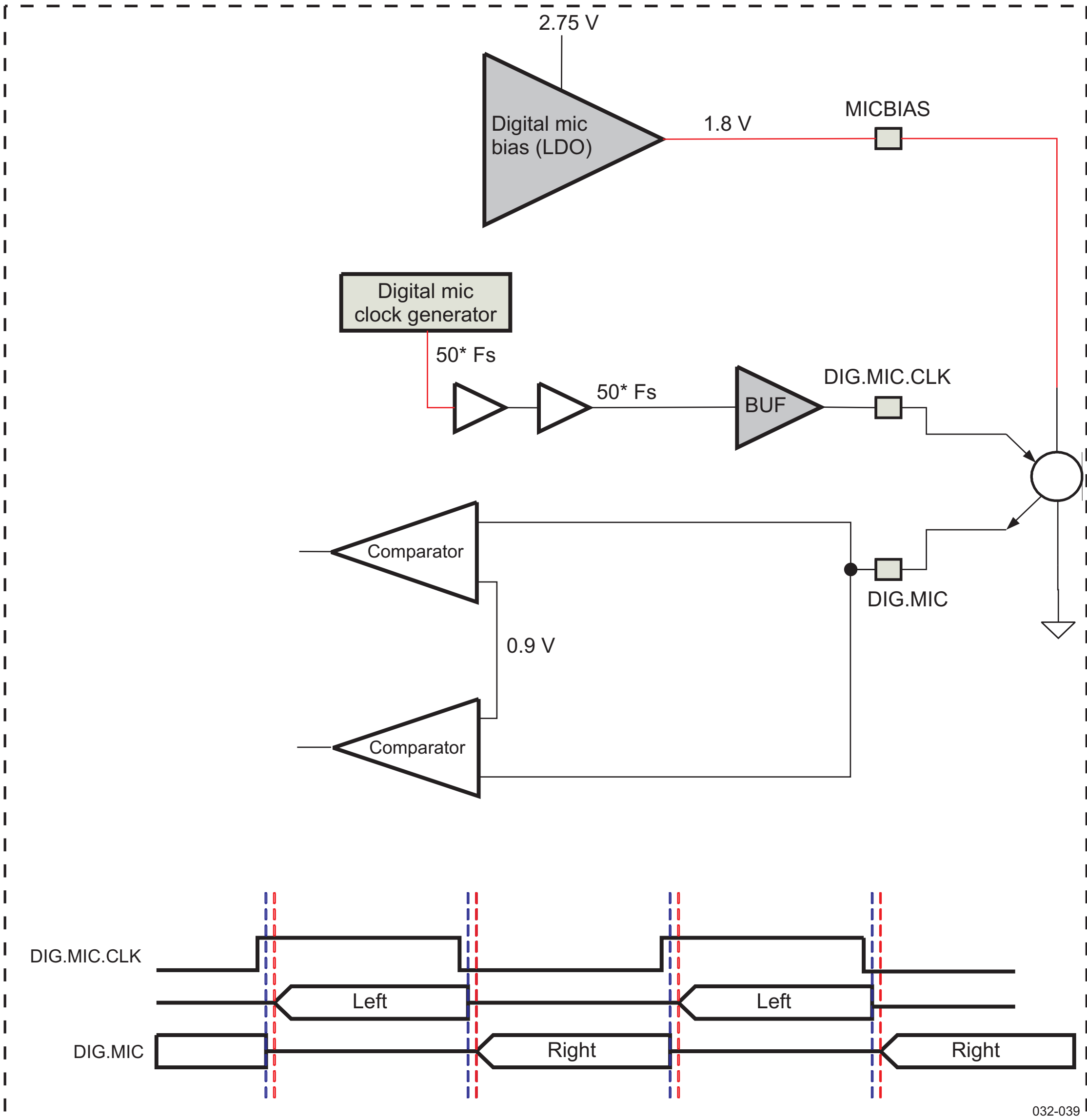


Figure 6-26. Example of PDM Interface Circuitry

6.2.6 Uplink Characteristics

Figure 6-27 shows the uplink amplifier. Table 6-21 lists the characteristics of the uplink amplifier.

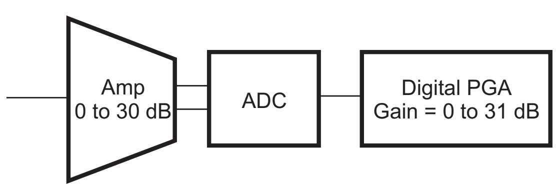


Figure 6-27. Uplink Amplifier

Table 6-21. Uplink Amplifier Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Speech delay	Voice path		0.5		ms
Gain range(1)		0		61	dB
Absolute gain	0 dBFs at 1.02 kHz	–1		1	dB
Peak-to-peak differential input voltage (0 dBFs)	For differential input 0 dB gain setting			1.5	V_{PP}
Peak-to-peak single-ended input voltage (0 dBFs)	For single-ended input 0 dB gain setting			1.5	V_{PP}
Input impedance(2)		40k		70k	Ω
Total harmonic distortion (sine wave at 1.02 kHz)	At –1 dBFs		–80	–75	dB
	At –6 dBFs		–74	–69	
	At –10 dBFs		–70	–65	
	At –20 dBFs		–60	–55	
	At –60 dBFs		–20	–15	
Idle channel noise	20 Hz to 20 kHz, A-weighted, gain = 0 dB		–85	–78	dBFs
	16 kHz: < 20 Hz to 7 kHz, gain = 0 dB		–90		
	8 kHz: P-weighted voice, gain = 18 dB		–87		
	16 kHz: < 20 Hz to 7 kHz, gain = 18 dB		–82		
Crosstalk A/D to D/A	Gain = 0 dB		–80		dB
Crosstalk path between two microphones		–70			dB
Intermodulation distortion	Two-tone method			–60	dB

(1) Gain range is defined by: Preamplifier = 0 to 30 dB; Filter = 0 to 31 dB (1-dB steps)
(2) Impedance varies in the specified range with gain selection.

6.2.7 Microphone Amplification Stage

Microphone amplification stages perform single-to-differential conversion for single-ended inputs. Two programmable gains from 0 to 30 dB can be set:

- Automatic level control for main microphone or submicrophone input. The gain step is 1 dB.
- Level control by register for line-in or carkit input, or headset microphone. The gain step is 6 dB.

The amplification stage outputs are connected to the ADC input (ADC left and right).

6.2.8 Carkit Input

The USB-CEA carkit uses the DP pad to input the audio signal.

The MCPC carkit uses the TXAF analog pad to input the audio signal.

Figure 6-28 shows the uplink carkit full path uplink characteristics for audio and USB.

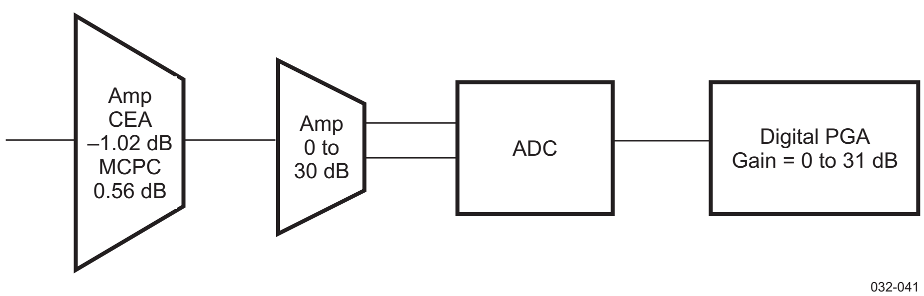


Figure 6-28. Carkit Input Uplink Path Characteristics

Table 6-22 lists the electrical characteristics of the MCPC and USB-CEA carkit audio.

Table 6-22. MCPC and USB-CEA Carkit Audio Uplink Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Gain range (1)		–1		60	dB
Absolute gain, 0 dBFs at 1.02 kHz (1) (2) (3)	USB-CEA default gain setting	–1.5		1.5	dB
	MCPC default gain setting	–1.5		1.5	
Speech delay	Voice path		0.5		ms
Input common mode voltage (4)	USB-CEA	1.3		1.9	V
Phone microphone amplifier input impedance at 1 kHz	USB-CEA	8	120		kΩ
	MCPC	5	100		
Peak-to-peak single-ended input voltage (0 dBFs)	Default setting			1.414	V_{PP}
Total harmonic distortion (sine wave at 1 kHz), default gain setting	At –1 dBFs		–74	–60	dB
	At –6 dBFs				
	At –10 dBFs				
	At –20 dBFs				
	At –60 dBFs				
THD + N (20 Hz to 20 kHz, A-weighted)	At 0 dBFs		60		dB
Signal noise ratio (20 Hz to 20 kHz, A-weighted)	At 0 dBFs		60		dB
Idle channel noise (20 Hz to 20 kHz, A-weighted), default gain setting	USB-CEA		–77		dBFs
	MCPC		–80	–77	
Output PSRR (20 Hz to 20 kHz, A-weighted)	USB-CEA		50		dB
	MCPC		35		

(1) Gain range is defined by: MCPC/CEA amplifier = 0.56 dB/–1.02 dB; Preamplifier = 0 to 30 dB; Filter = 0 to 31 dB (1-dB steps).
(2) The CEA default gain setting assumes 0 dB on the preamplifier, 1 dB on the digital filter, and the MCPC/CEA amplifier at –1.02 dB.
(3) The MCPC default gain setting assumes 0 dB on the preamplifier, 0 dB on the digital filter, and the MCPC/CEA amplifier at 0.56 dB.
(4) Full-scale input voltage is 1 V minimum.

6.2.9 Digital Audio Filter Module

Figure 6-29 shows the digital audio filter uplink full path characteristics for the audio interface.

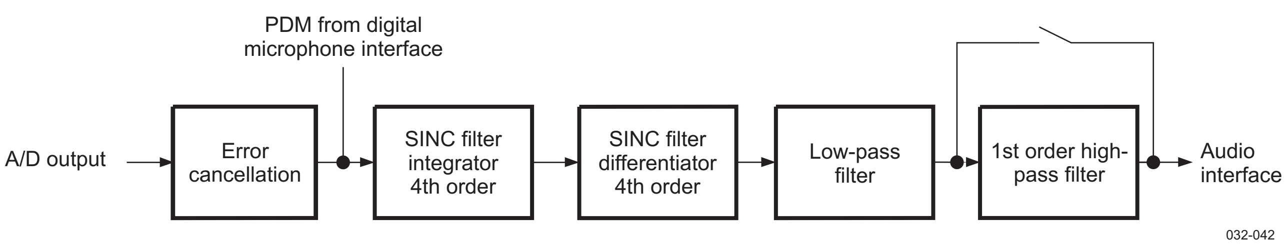


Figure 6-29. Digital Audio Filter Uplink Path Characteristics

The HPF can be bypassed. It is controlled by the MISC_SET_2 ATX_HPF_BYP bit, address 0x49.

Table 6-23 lists the audio filter frequency responses relative to reference gain at 1 kHz.

Table 6-23. Digital Audio Filter TX Electrical Characteristics

Parameter	Test Conditions	Min	Typ	Max	Unit
Passband		0.0005		0.42	F_S
Passband gain	In region 0.0005*F_S to 0.42*F_S (1)	–0.25		0.25	dB
Stopband			0.6		F_S
Stopband attenuation	In region 0.6*F_S to 1*F_S (1)		60		dB
Group delay			15.8/F_S		μs

(1) F_S is the sampling frequency (8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz).

6.2.10 Digital Voice Filter Module

Figure 6-30 shows the digital voice filter uplink full path characteristics of the voice interface.

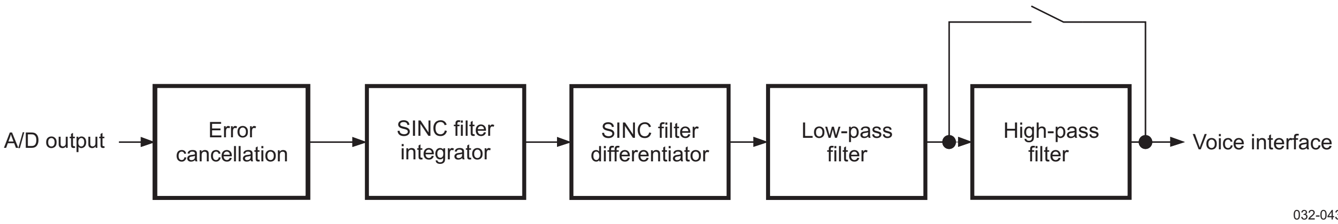


Figure 6-30. Digital Audio Filter Uplink Path Characteristics

The global HPF or only the third-order HPF can be bypassed (when the third-order HPF is skipped, the first-order HPF remains active). It is controlled by the MISC_SET_2 VTX_3RD_HPF_BYP bit, address 0x49, the for the third-order HPF, and by the VTX_HPF_BYP bit for the global HPF.

6.2.10.1 Voice Uplink Filter (Sampling Frequency at 8 kHz)

Figure 6-31 and Figure 6-32 show the voice uplink frequency response with a sampling frequency of 8 kHz.

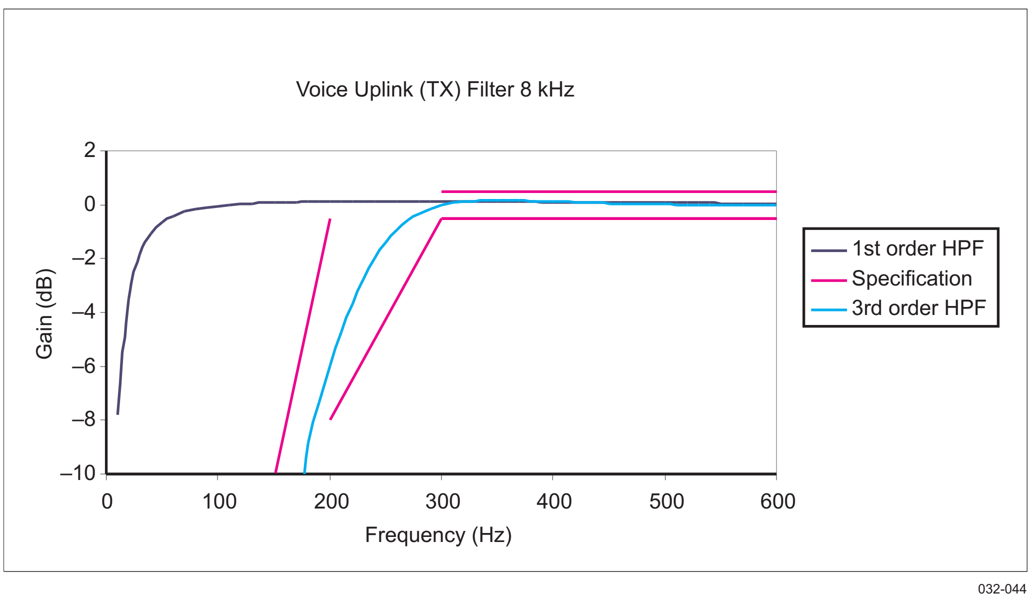
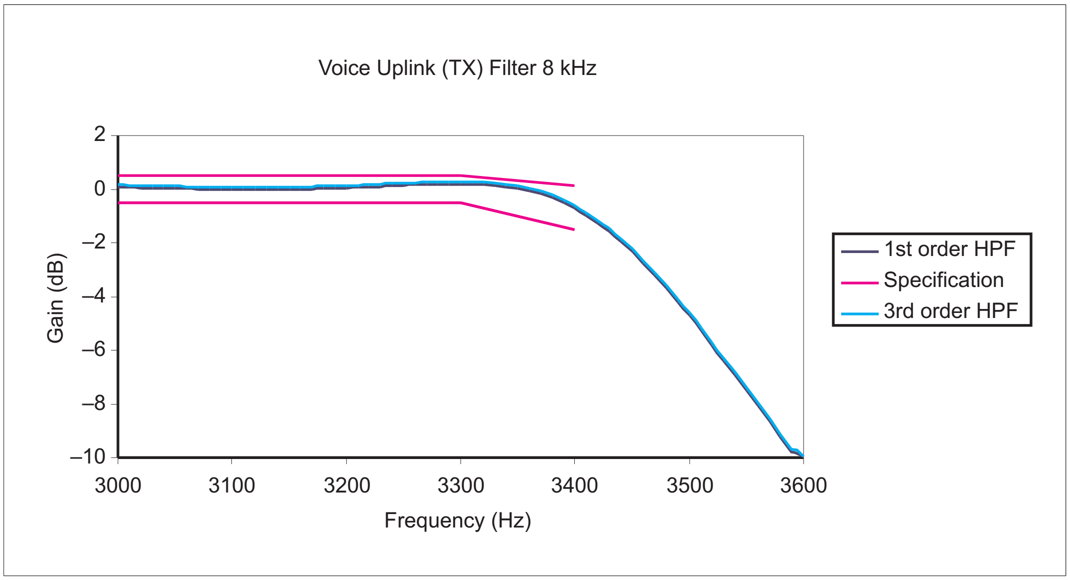


Figure 6-31. Voice Uplink Frequency Response With F_S = 8 kHz (Frequency Range 0 to 600 Hz)



032-045

Figure 6-32. Voice Uplink Frequency Response With F_S = 8 kHz (Frequency Range 3000 to 3600 Hz)

Table 6-24 lists the voice filter frequency responses relative to reference gain at 1 kHz with F_S = 8 kHz.

Table 6-24. Digital Voice Filter TX Electrical Characteristics With F_S = 8 kHz

Parameter	Test Conditions	Min	Typ	Max	Unit
Frequency response relative to reference gain at 1 kHz	100 Hz			–20	dB
	200 Hz	–8		–0.5	
	300 to 3300 Hz	–0.5	0	0.5	
	3400 Hz	–1.5	0	0.1	
	4000 Hz			–17	
	4600 Hz			–40	
	>6000 Hz			–45	
Pole when HPF is disabled (first-order HPF)			24		Hz
Group delay			0.5		ms

6.2.10.2 Voice Uplink Filter (Sampling Frequency at 16 kHz)

Figure 6-33 and Figure 6-34 show the voice uplink frequency response with a sampling frequency of 16 kHz.

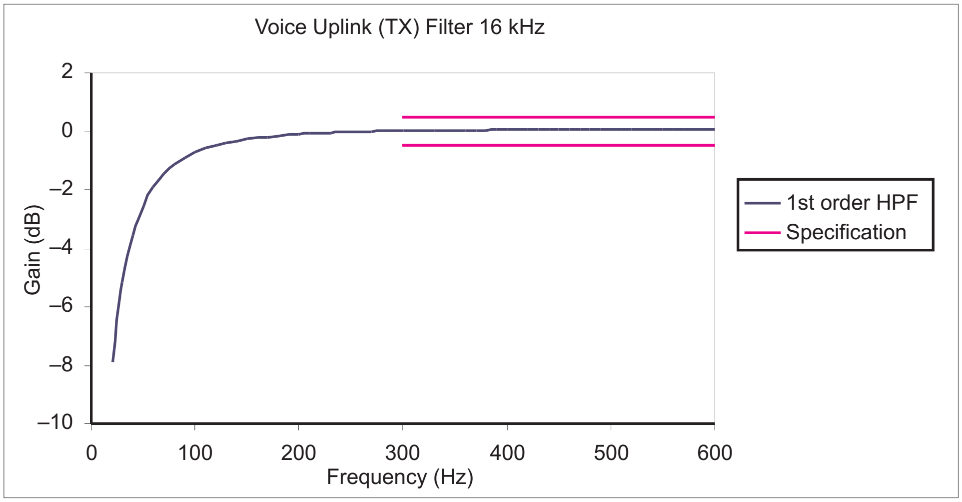


Figure 6-33. Voice Uplink Frequency Response With F_S = 16 kHz (Frequency Range 0 to 600 Hz)

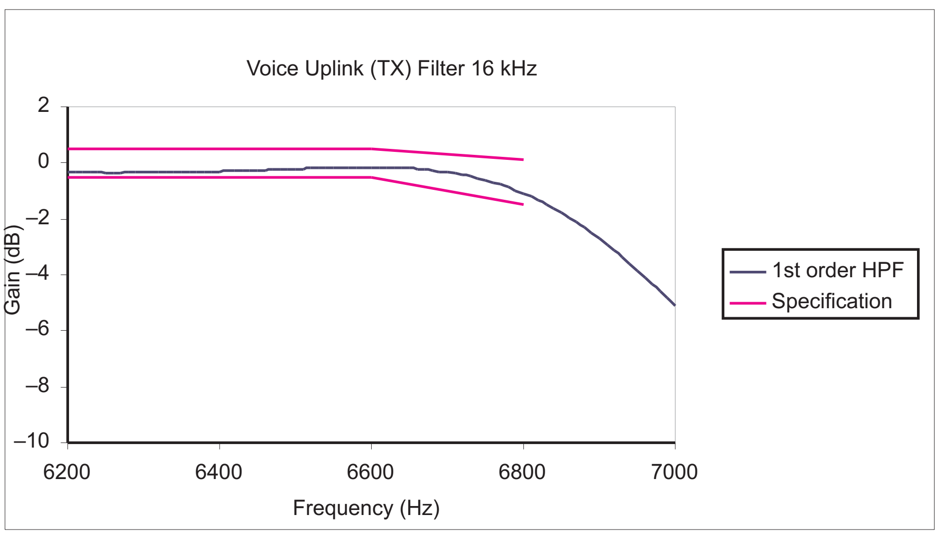


Figure 6-34. Voice Uplink Frequency Response With F_S = 16 kHz (Frequency Range 6200 to 7000 Hz)

Table 6-25 lists the voice filter frequency responses relative to reference gain at 1 kHz with F_S = 16 kHz.

Table 6-25. Digital Voice Filter TX Electrical Characteristics With F_S = 16 kHz

Parameter	Test Conditions	Min	Typ	Max	Unit
Frequency response relative to reference gain at 1 kHz (first-order HPF)	300 to 6600 Hz	–0.5		0.5	dB
	6800 Hz	–1.5		0.1	
	8000 Hz	–0.5	0	–17	
	9200 Hz	–1.5	0	–40	
	12000 Hz			–45	

Table 6-25. Digital Voice Filter TX Electrical Characteristics With F_S = 16 kHz (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Pole when third-order HPF is disabled (first-order HPF)			47		Hz

7 USB HS 2.0 OTG Transceiver

The TPS65950 includes a USB OTG transceiver with CEA and MCPC carkit interfaces that support USB 480 Mbps HS, 12 Mbps full-speed (FS), and USB 1.5 Mbps low-speed (LS) through a 4-pin ULPI.

The carkit block ensures the interface between the phone and a carkit device. The TPS65950 USB supports CEA and MCPC carkit standards.

Figure 7-1 is a block diagram of the USB 2.0 physical layer (PHY).

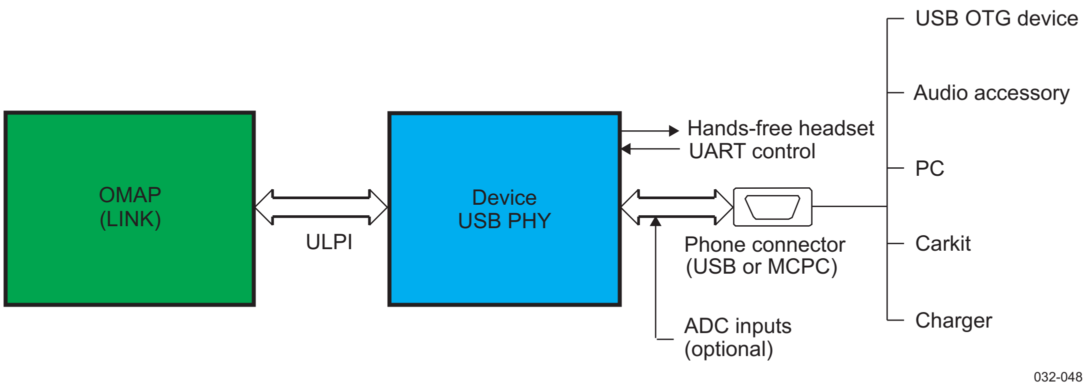


Figure 7-1. USB 2.0 PHY Overview

7.1 USB Features

The device has a USB OTG carkit transceiver that allows system implementation that complies with the following specifications:

- *Universal Serial Bus 2.0 Specification*
- *On-The-Go Supplement to the USB 2.0 Specification*
- *CEA-2011: OTG Transceiver Interface Specification*
- *CEA-936A: Mini-USB Analog Carkit Interface Specification*
- *MCPC ME-UART GL-006 Specification*
- *UTMI+ Low Pin Interface Specification*

The features of the individual specifications are:

- *Universal Serial Bus 2.0 Specification* (hereafter referred to as the USB 2.0 specification):
  - 5-V-tolerant data line at HS/FS, FS-only, and LS-only transmission rates
  - 7-V-tolerant video bus (VBUS) line
  - Integrated data line serial termination resistors (factory-trimmed)
  - Integrated data line pullup and pulldown resistors
  - On-chip 480-MHz PLL from the internal system clock (19.2, 26, and 38.4 MHz)
  - Synchronization (SYNC)/end-of-period (EOP) generation and checking
  - Data and clock recovery from the USB stream
  - Bit-stuffing/unstuffing and error detection
  - Resume signaling, wakeup, and suspend detection
  - USB 2.0 test modes
- *On-The-Go Supplement to the USB 2.0 Specification* (hereafter referred to as the OTG supplement to the USB 2.0 specification):
  - 3-pin LS/FS serial mode (DAT_SE0)
  - 4-pin LS/FS serial mode (VP_VM)
- *CEA-2011: OTG Transceiver Interface Specification*:

  - 3-pin LS/FS serial mode (DAT_SE0)
  - 4-pin LS/FS serial mode (VP_VM)
- *CEA-936A: Mini-USB Analog Carkit Interface Specification* (hereafter referred to as the CEA-936A specification):
  - 5-pin CEA mini-USB analog carkit interface
  - UART signaling
  - Audio (mono/stereo) signaling
  - UART transactions during audio signaling
  - Basic and smart 4-wire/5-wire carkit, chargers, and accessories
  - ID CEA resistor comparators
- *MCPC ME-UART GL-006 Specification* (hereafter referred to as the MCPC ME-UART specification):
  - 11-pin MCPC Association of Radio Industries and Businesses (ARIB)-USBi (USB interface standard) analog carkit interface
  - UART signaling
- *UTMI+ Low Pin Interface Specification* (hereafter referred to as the ULPI specification):
  - 12-pin ULPI with 8-pin parallel data for USB signaling and register access
  - 60-MHz clock generation
  - Register mapping

7.2 USB Transceiver

Figure 7-2 is an application schematic of the USB system.

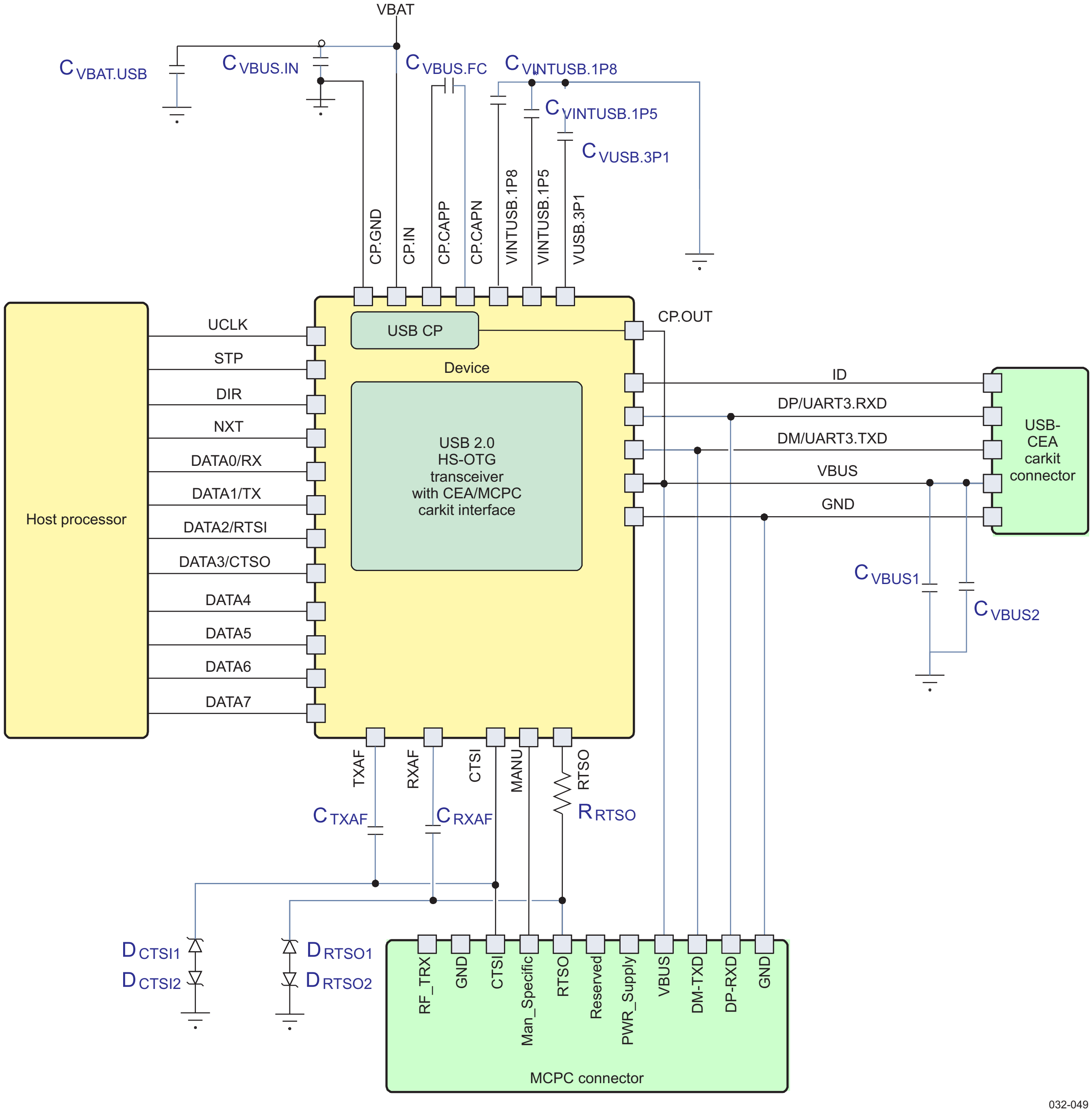


Figure 7-2. USB System Application Schematic

NOTE

For the component values, see Table 15-1.

7.2.1 MCPC Carkit Port Timing

MCPC UART specification:

- 11-pin MCPC ARIB-USBI analog carkit interface
- Integrated 50 RRTSO resistor
- UART signaling (from 600 bps to 460.8 kbps)
- Audio (mono/stereo) signaling: In this mode, the ULPI data bus is redefined as a 4-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

The UART data are sent and received on the USB D+/D– pads, and the handshake signals are sent and received on the RTSO/CTSI pads.

Figure 7-3 shows the MCPC UART and handshake mode data flow.

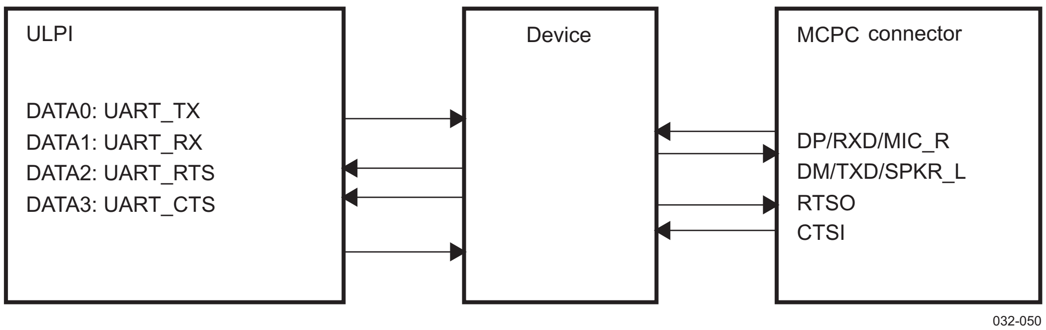


Figure 7-3. MCPC UART and Handshake Mode Data Flow

Table 7-1 lists the McPC UART and handshake mode timings.

Table 7-1. MCPC UART and Handshake Mode Timings

Notation	Parameter		Min	Max	Unit
CK5	$t_{d(UART_TXH-DM)}$	Delay time, UART_TX rising edge to DM transition	10	37	ns
CK6	$t_{d(UART_TXL-DM)}$	Delay time, UART_TX falling edge to DM transition	2.5	13	ns
CK7	$t_{d(DPH-UART_RX)}$	Delay time, DP rising edge to UART_RX transition	17	40	ns
CK8	$t_{d(DPL-UART_RX)}$	Delay time, DP falling edge to UART_RX transition	26	50	ns
CK9	$t_{d(UART_CTSH-RTSO)}$	Delay time, UART_CTS rising edge to RTSO transition	1	18	ns
CK10	$t_{d(UART_CTSL-RTSO)}$	Delay time, UART_CTS falling edge to RTSO transition	1	18	ns
CK11	$t_{d(CTSIH-UART_RTS)}$	Delay time, CTSI rising edge to UART_RTS transition	3	16	ns
CK12	$t_{d(CTSIL-UART_RTS)}$	Delay time, CTSI falling edge to UART_RTS transition	3	16	ns

Figure 7-4 shows the MCPC UART and handshake mode timings.

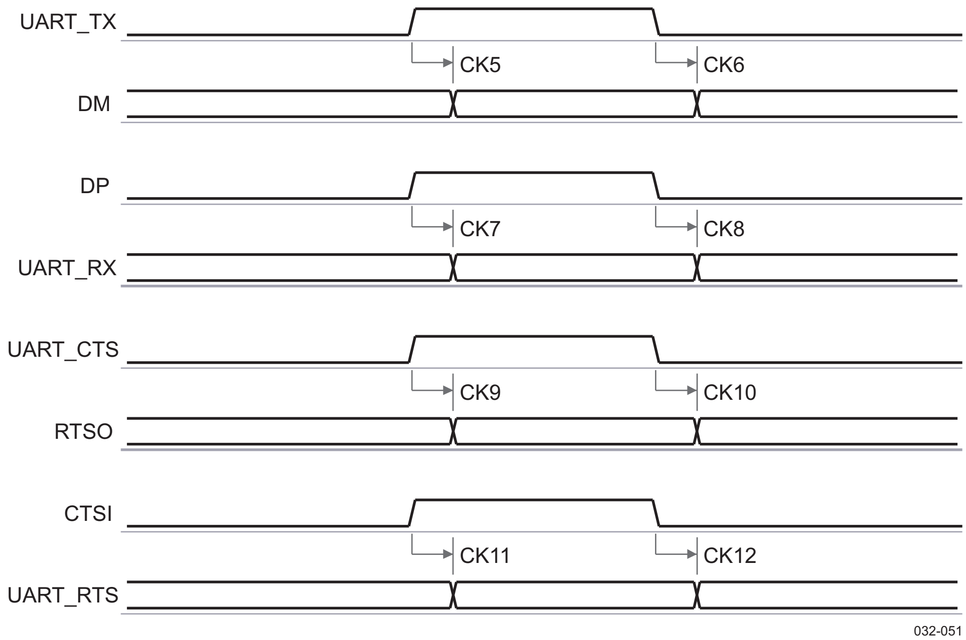


Figure 7-4. MCPC UART and Handshake Mode Timings

7.2.2 USB-CEA Carkit Port Timing

CEA carkit mode lets the link communicate through the USB PHY to a remote carkit in CEA audio + data during audio (DDA) mode as defined in the CEA-936A specification. In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

UART data are sent and received on the USB D+/D– pads. D+/D– are also used in this mode to carry audio I/O signals.

Table 7-2 assumes testing over the recommended operating conditions (see the CEA-936A specification).

Table 7-2. USB-CEA Carkit Interface Timing Parameters

Parameter		Min	Max	Unit
$t_{PH_DP_CON}$	Phone D+ connect time	100		ms
$t_{CR_DP_CON}$	Carkit D+ connect time	150	300	ms
$t_{PH_DM_CON}$	Phone D– connect time		10	ms
$t_{PH_CMD_DLY}$	Phone command delay	2		ms
$t_{PH_MONO_ACK}$	Phone mono acknowledge		10	ms
$t_{PH_DISC_DET}$	Phone D+ disconnect time	150		ms
$t_{CR_DISC_DET}$	Carkit D– disconnect detect	50	150	ms
$t_{PH_AUD_BIAS}$	Phone audio bias	1		ms
$t_{CR_AUD_DET}$	Carkit audio detect	400	800	μs
$t_{CR_UART_DET}$	Carkit UART detect (DDA enabled)	700	1200	ns
$t_{PH_STLO_DET}$	Phone stereo D+ low detect	30	100	ms
$t_{PH_PLS_POS}$	Phone D– interrupt pulse width	200	600	ns
$t_{CR_PLS_NEG}$	Carkit D+ interrupt pulse width	200	600	ns
$t_{DAT_AUD_POL}$	DDA polarity	20	60	ms
$t_{ACC_COL_DET}$	Accessory identification (ID) collision detect	2	3	ms

Table 7-2. USB-CEA Carkit Interface Timing Parameters (continued)

Parameter		Min	Max	Unit
$t_{ACC_INT_PW}$	Accessory ID interrupt pulse width	200	400	µs
$t_{ACC_INT_WAIT}$	Accessory ID interrupt wait time	10	15	ms
$t_{ACC_CMD_WAIT}$	Accessory ID command wait time	0		ms
$t_{PH_INT_PW}$	Phone ID interrupt pulse width	4	8	ms
$t_{PH_INT_WAIT}$	Phone ID interrupt wait time	4	8	ms
$t_{PH_CMD_WAIT}$	Phone ID command wait time	0		ms
$t_{PH_UART_RPT}$	Phone command repeat time	50		ms
$t_{CR_UART_RSP}$	Carkit UART response		30	ms
$t_{CR_INT_RPT}$	Carkit interrupt repeat time	50		ms
f_{UART_DFLT}	Default UART signaling rate (typical rate)		9600	bps

Figure 7-5 shows the USB-CEA carkit UART data flow.

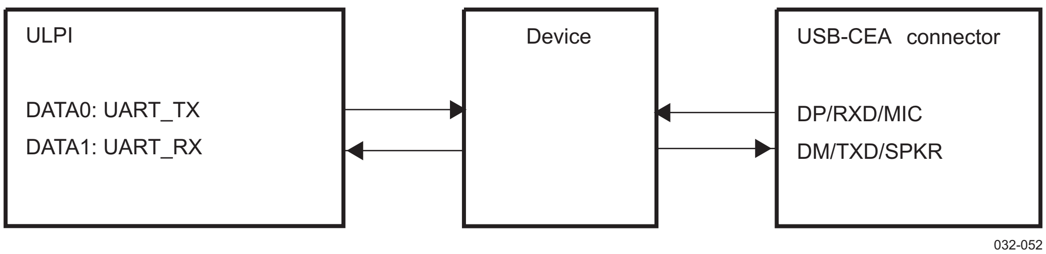


Figure 7-5. USB-CEA Carkit UART Data Flow

Table 7-3 lists the USB-CEA carkit UART timing parameters.

Table 7-3. USB-CEA Carkit UART Timing Parameters

Notation	Parameter			Min	Max	Unit
CK1	$t_{d(UART_TXH-DM)}$	Delay time, UART_TX rising edge to DM transition		4.0	11	ns
CK2	$t_{d(UART_TXL-DM)}$	Delay time, UART_TX falling edge to DM transition		4.0	11	ns
CK3	$t_{d(DPH-UART_RX)}$	Delay time, DP rising edge to UART_RX transition	At 38.4 MHz	205	234	ns
			At 19.2 MHz	310	364	
CK4	$t_{d(DPL-UART_RX)}$	Delay time, DP falling edge to UART_RX transition	At 38.4 MHz	205	234	ns
			At 19.2 MHz	310	364	

Figure 7-6 shows the USB-CEA carkit UART timings.

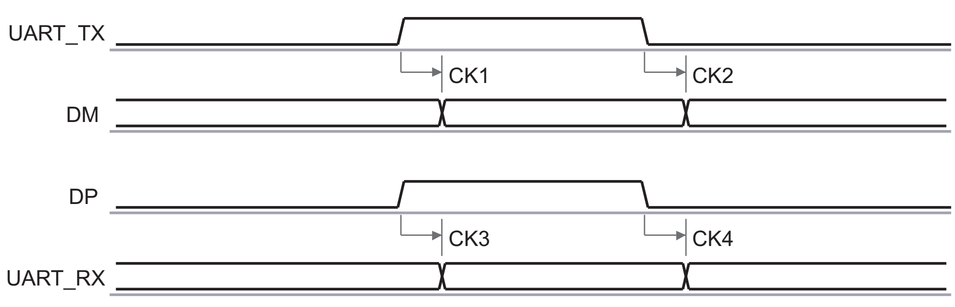


Figure 7-6. USB-CEA Carkit UART Timing Parameters

7.2.3 HS USB Port Timing

The ULPI interface supports an 8-bit data bus and the internal clock mode. The 4-bit data bus and the external clock mode are not supported.

The HS functional mode supports an operating rate of 480 Mbps.

Table 7-4 and Table 7-5 assume testing over the recommended operating conditions (see Figure 7-7).

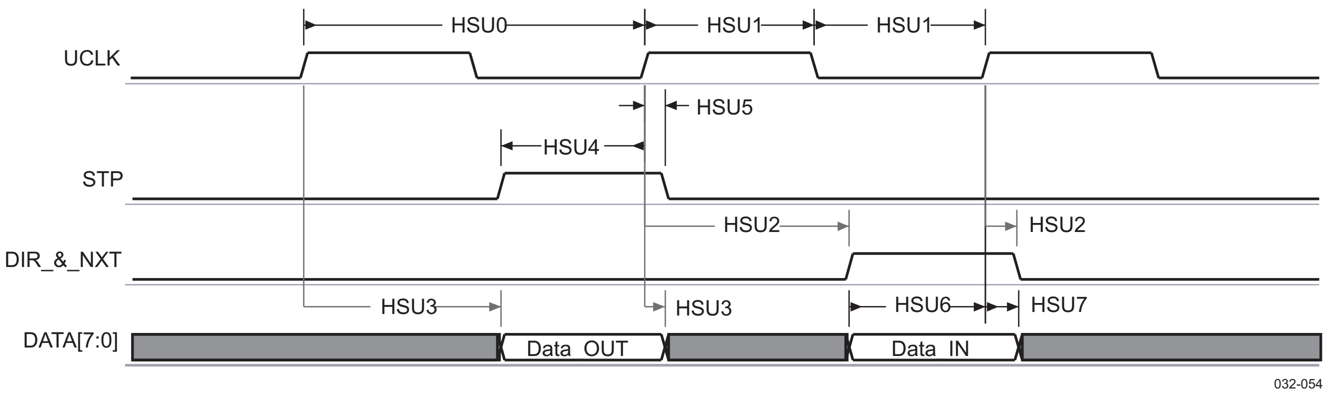


Figure 7-7. HS USB Interface—Transmit and Receive Modes (ULPI 8-Bit)

NOTE

ULPI data [7:0] lines are set to 1 after USB PHY power up, and before the clock signal is stable.

The input timing requirements are given by considering a rising or falling time of 1 ns.

Table 7-4. HS USB Interface Timing Requirement Parameters

Notation	Parameter		Min	Max	Unit
HSU4	$t_{s(STPV-CLKH)}$	Setup time, STP valid before UCLK rising edge	6		ns
HSU5	$t_{h(CLKH-STPIV)}$	Hold time, STP valid after UCLK rising edge	0		ns
HSU6	$t_{s(DATAV-CLKH)}$	Setup time, DATA[0:7] valid before UCLK rising edge	6		ns
HSU7	$t_{h(CLKH-DATIV)}$	Hold time, DATA[0:7] valid after UCLK rising edge	0		ns

Table 7-5. HS USB Interface Switching Requirement Parameters(1)

Notation	Parameter			Min	Typ	Max	Unit
HSU0	$f_{p(CLK)}$	UCLK clock frequency	Steady state	58.42	60	61.67	MHz
HSU1	$t_{W(CLK)}$	UCLK duty cycle	Steady state	48.3%	50%	51.7%	
HSU2	$t_{d(CLKH-DIR)}$	Delay time, UCLK rising edge to DIR transition	Steady state	0		9	ns
	$t_{d(CLKH-NXTV)}$	Delay time, UCLK rising edge to NXT transition	Steady state	0		9	ns
HSU3	$t_{d(CLKH-DATV)}$	Delay time, UCLK rising edge to DATA[0:7] transition	Steady state	0		9	ns

(1) The capacitive load for output data and control load is 10 pF (rising and falling time is 2 ns).
The capacitive load for the CLK port is 6 pF (rising and falling time is 1 ns).
The HS USB interface has only one state: steady state.

7.2.4 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It contains the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through UTMI.

There are two main classes of transmitters and receivers in the PHY:

- FS and LS transceivers. These are the legacy USB1.x transceivers.
- HS transceivers

To bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A digital phase-locked loop (DPLL) that does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB, and the clock required for the switched capacitor resistance block
- A switched capacitor resistance block that replicates an external resistor on chip

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

The PHY also contains circuitry that protects it from an accidental 5-V short on the DP and DM lines and from 8-kV IEC ESD strikes.

7.2.4.1 5-V Tolerance

When the voltage on DP or DM exceeds 3.6 V, a stress condition is detected. In this case, the current is drawn from the DP/DM line, to prevent damage caused by the stress voltage. In this condition, the VRUSB_3V supply can be charged as high as 3.6 V. Table 7-6 lists the tolerances.

Table 7-6. 5V-Tolerant Electrical Summary

Parameter		Comments	Min	Typ	Max	Unit
Continuous short-circuit stress	DCSTRESS	50% TX/50% RX/50% LS/50% FS/VBUS = 5.25 V	24			h
Worst case overshoot and undershoot stress	ACSTRESS	t_{HI} = 60 ns/t_{LO} = 100 ns/t_R = t_F = 4 ns/ V_{HI} = 4.6 V/VLO = –1.0 V/R_{SRC} = 39Ω/ 50% TX/50% RX/VBUS = 5.25 V	24			h
Internal DP/DM stress voltage	VDX_STRESS	Force 5.25 V VBUS/DP/DM			4.3	V
V3P1 stress voltage	V3P1_STRESS	Force 5.25 V VBUS/DP/DM/ID			3.6	V
DP/DM input stress current	IDX_STRESS	Force 5.25 V VBUS/DP/DM	30			mA
ID input stress current	IID_STRESS	Force 5.25 V VBUS/DP/DM/ID			25	µA

7.2.4.2 LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines D+/–. The main purpose of the single-ended receivers is to qualify the D+ and D– signals in the FS/LS modes of operation. Table 7-7 lists the parameters of the LS/FS single-ended receivers.

Table 7-7. LS/FS Single-Ended Receivers

Parameter		Comments	Min	Typ	Max	Unit
USB Single-Ended Receivers						
Skew between VP and VM	SKWVP_VM	Driver outputs unloaded	–2	0	2	ns
Single-ended hysteresis	V_{SE_HYS}			0		mV
High (driven)	V_{IH}		2			V
Low	V_{IL}				0.8	V
Switching threshold	V_{TH}		0.8		2	V

Table 7-7. LS/FS Single-Ended Receivers (continued)

Parameter		Comments	Min	Typ	Max	Unit
UART Receiver CEA						
	VIH_SER	DP_PULLDOWN asserted	2			V
Serial interface input low	VIL_SER	DP_PULLDOWN asserted			0.8	V
Switching threshold	V_{TH}		0.8		2	V
UART Receiver MCPC From DP.RXD						
MCPC DP pullup	RMCPCDP	Internal pullup	4.7k		10k	Ω
Open-drain input high level	Z_{IH}	Internal MCPC DP pullup asserted		Open		Ω
Open-drain input low level	Z_{IL}	External open-drain NMOS impedance to ground. With internal MCPC DP pullup asserted.			100	Ω
Output high level	V_{OH} (*)	At DATA1 pin	VIO – 0.45			V
Output low level	V_{OL}	At DATA1 pin			0.45	V

7.2.4.3 LS/FS Differential Receiver

A differential input receiver (RX) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted to digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit that recovers the clock from the data. In an additional serial mode, the differential data is directly output on the RXRCV pin. Table 7-8 lists the parameters of the LS/FS differential receiver.

Table 7-8. LS/FS Differential Receiver

Parameter		Comments	Min	Typ	Max	Unit
Skew between VP/VM	SKWVP_VM	Driver outputs unloaded	–16	0	16	ns
Receiver power-up time	TPWR_UP_RCV		0	100	200	μs
Differential common mode range	V_{CM}		0.8		2.5	V
Differential input sensitivity	V_{DI}		0.2			V

7.2.4.4 LS/FS Differential Transmitter

The USB transceiver (TX) uses a differential output driver to drive the USB data signal D+/– onto the USB cable. The driver outputs support 3-state operation to achieve bidirectional half-duplex transactions. Table 7-9 lists the parameters of the LS/FS differential transmitter.

Table 7-9. LS/FS Differential Transmitter

Parameter		Comments	Min	Typ	Max	Unit
B-device (dual-role) unconfigured average current	IB_OTG_UNCFG	0 V = VBUS = 5.25 V, t_{AVG} = 1 ms			150	μA
B-device (secure remote password [SRP] capable, peripheral only) unconfigured average current	IB_PO_UNCFG				8	mA
FS fall time/rise time	t_{Ff}, t_{Fr}	10%–90% C_L = 50 pF on DP and DM	4		20	ns
FS rise and fall time matching	TFRFM	10%–90% C_L = 50 pF on DP and DM	90%		110%	
FS width of SE0 interval during differential transition	t_{Fst}	Pulldowns R = 15 kΩ on DP and DM Pullup R = 1.5 kΩ at 3.6 V on DP only			14	ns
LS fall time/rise time	t_{LF}, t_{LR}	10%–90% C_L = [200–600] pF on DP and DM Pullup R = 1.5 kΩ at 3.6 V for DM only	75		300	ns
LS rise and fall time matching	TLRFM	10%–90% C_L = [200–600] pF on DP and DM Pullup R = 1.5 kΩ at 3.6 V for DM only	80%		120%	

Table 7-9. LS/FS Differential Transmitter (continued)

Parameter		Comments	Min	Typ	Max	Unit
LS width of SE0 interval during differential transition	t_{LST}	Pulldowns R = 15 kΩ on DP and DM Pullup R = 1.5 kΩ at 3.6 V on DM only			210	ns
Driver power-up time	TPWR_UP_TXD	Pulldowns R = 15 kΩ on DP and DM Pullup R = 1.5 kΩ at 3.6 V on DM only	0	100	200	µs
FS source driver jitter to next transition	t_{SDJ1}	C_L = 50 pF on DP and DM	–2		2	ns
FS source driver jitter for paired transitions	t_{SDJ2}	C_L = 50 pF on DP and DM	–1		1	ns
LS upstream facing port source driver jitter (next transition)	t_{USDJ1}	C_L = [200–600] pF on DP and DM Pullup R = 1.5 kΩ at 3.6 V for DM only	–25		25	ns
LS upstream facing port source driver jitter (next transition)	t_{USDJ2}	C_L = [200–600] pF on DP and DM Pullup R = 1.5 kΩ at 3.6 V for DM only	–10		10	ns
Output signal cross-over voltage	Vcrs	Pulldowns R = 15 kΩ on DP and DM Pullup R = 1.5 kΩ at 3.6 V on DM only	1.3		2	V
High (driven)	V_{OH}	Pulldowns R = 15 kΩ on DP and DM	2.8	3.3	3.6	V
Low	V_{OL}	Pullups R = 1.5 kΩ at 3.6 V on DP and DM	0	0.1	0.3	V
Driver output resistance	Z_{DRV}/R_S		28	36	44	Ω

7.2.4.5 HS Differential Receiver

The HS receiver consists of the following blocks:

- A differential input comparator to receive the serial data
- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a nonreturn to zero inverted (NRZI) decoder, bit unstuffing, and a serial-to-parallel converter to generate the UTMI DATAOUT

Table 7-10 lists the parameters of the HS differential receiver.

Table 7-10. HS Differential Receiver

Parameter		Comments	Min	Typ	Max	Unit
Input Levels for HS						
HS squelch detection threshold	V_{HSSQ}	(Differential signal amplitude)	100	125	150	mV
HS disconnect detection threshold	V_{HSDSC}	(Differential signal amplitude)	525	600	625	mV
HS data signaling common mode voltage range	V_{HSCM}		–50	200	500	mV
HS differential input sensitivity	V_{DIHS}	(Differential signal amplitude)	–100		100	mV
Input Impedance for HS						
Internal specification for input capacitance	C_{HSLOAD}			11		pF
Internal C_{HSLOAD} DP/DM matching	$C_{HSLOADM}$			0.2		pF
External Components With the Total Budget Combined (Without USB Cable Load)						
External capacitance on DP or DM					2	pF
External series resistance on DP or DM					1	Ω

7.2.4.6 HS Differential Transmitter

The HS transmitter is always operated on the UTMI parallel interface. The parallel data on the interface is serialized, bit-stuffed, NRZI-encoded, and transmitted as a dc output current on DP or DM, depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double, thereby doubling the differential amplitude seen on the DP/DM lines.

Table 7-11 lists the parameters of the HS differential transmitter.

Table 7-11. HS Differential Transmitter

Parameter		Comments	Min	Typ	Max	Unit
Output Levels for HS						
HS TX idle level	V_{HSOI}	Absolute voltage DP/DM – Both internal/external 45 Ω	–10	0	10	mV
HS TX data signaling high	V_{HSOH}	Absolute voltage DP/DM – Both internal/external 45 Ω	360	400	440	mV
HS data signaling low	V_{HSOL}		–10	0	10	mV
Chirp J level	V_{CHIRPJ}	Differential voltage	700	800	1100	mV
Chirp K level	V_{CHIRPK}	Differential voltage	–900	–800	–500	mV
HS TX disconnect threshold	$V_{DISCOUT}$	Absolute voltage DP/DM—No external 45 Ω	700			mV
Driver Characteristics						
Rise time	t_{HSR}	(10%–90%)	500			ps
Fall time	t_{HSF}	(10%–90%)	500			ps
Driver output resistance	Z_{HSDRV}	Also serves as HS termination	40.5	45	49.5	Ω

7.2.4.7 CEA/MCPC/UART Driver

Table 7-12 lists the parameters of the CEA/MCPC/UART driver.

Table 7-12. CEA/MCPC/UART Driver

Parameter		Comments	Min	Typ	Max	Unit
UART Driver CEA						
Phone UART edge rates	$t_{PH_UART_EDGE}$	DP_PULLDOWN asserted			1	µs
Serial interface output high	V_{OH_SER}	ISOURCE = 4 mA	2.4	3.3	3.6	V
Serial interface output low	V_{OL_SER}	ISINK = –4 mA	0	0.1	0.4	V
UART Driver MCPC to DM.TX.						
Input high level	V_{IH} (*)	At DATA0 pin	VIO – 0.45			V
Input low level	V_{IL}	At DATA0 pin			0.45	V
MCPC DM external pullup	R_{MCPCDM}	External pullup	4.7k		10k	Ω
MCPC DM pullup supply	MCPCVDDEXT	External pullup supply	1.8		3.3	V
Open-drain output high level	Z_{OH}	External pullup asserted HiZ means high impedance equivalent to open		HiZ		Ω
Open-drain output low level	V_{OL}	With open-drain NMOS to ground is ON and external pullup is asserted.	0		0.6	V
Carkit Pulse Driver						
Pulse match tolerance	QPLS_MTCH	ZCR_SPKR_IN = 60 kΩ at f = 1 kHz			5%	
Phone D– interrupt pulse width	$t_{PH_PLS_POS}$	ZCR_SPKR_IN = 60 kΩ at f = 1 kHz	200		600	ns
Phone positive pulse voltage	$V_{PH_PLS_POS}$	ZCR_SPKR_IN = 60 kΩ at f = 1 kHz	2.8		3.6	V

7.2.4.8 Pullup/Pulldown Resistors

Table 7-13 lists the parameters of the pullup/pulldown resistors.

Table 7-13. Pullup/Pulldown Resistors

Parameter		Comments	Min	Typ	Max	Unit
Pullup Resistors						
Bus pullup resistor on upstream port (idle bus)	R_{PUI}	Bus idle	0.9	1.1	1.575	kΩ
Bus pullup resistor on upstream port (receiving)	R_{PUA}	Bus driven/driver outputs unloaded	1.425	2.2	3.09	kΩ
High (floating)	V_{IHZ}	Pullups/pulldowns on DP and DM lines	2.7		3.6	V
Phone D+ pullup voltage	$V_{PH_DP_UP}$	Driver outputs unloaded	3	3.3	3.6	V
Pulldown Resistors						
Phone D+/– pulldown	$R_{PH_DP_DWN}$ $R_{PH_DM_DWN}$	Driver outputs unloaded	14.25	18	24.8	kΩ
High (floating)	V_{IHZ}	Pullups/pulldowns on DP and DM lines	2.7		3.6	V
D+/– Data Line						
Upstream facing port	C_{INUB}			22	75	pF
OTG device leakage	$V_{OTG_DATA_LKG}$				0.342	V
Input impedance exclusive of pullup/pulldown (1)	Z_{INP}	Driver outputs unloaded (waiver from usb.org standards committee)	80	120		kΩ

(1) Waiver received from usb.org standards committee on ZINP 300kmin specification

7.2.4.9 PHY DPLL Electrical Characteristics

USB DPLL supports input frequencies of 12, 13, 19.2, 24, and 26 MHz. The input frequency must be programmed through frequency select bits. USB DPLL provides a low jitter and gives eight equidistant phases of the 480-MHz clock for the USB receiver.

Table 7-14 lists the electrical characteristics of the PHY DPLL.

Table 7-14. PHY DPLL Electrical Characteristics

Parameter		Comments	Min	Typ	Max	Unit
Input clock				12		MHz
				13		
				19.2		
				24		
				26		
Digital supply	VINTDIG		1.35	1.5	1.65	V
Analog 1.5-V supply	VRUSB_1V5		1.35	1.5	1.65	V
Analog 1.8-V supply	VRUSB_1V8		1.62	1.8	1.98	V
Output frequency (eight phases)				480		MHz
RMS period jitter (output)					10	ps
Deterministic period jitter (output)					50	ps
RMS jitter per phase noise frequency band (input)		Frequency band: 1 to 10 Hz			310	ps
		Frequency band: 10 to 100 Hz			90	
		Frequency band: 100 to 1000 Hz			30	
		Frequency band: 1 to 10 kHz			10	
		Frequency band: 10 to 100 kHz			10	
		Frequency band: 0.1 to 0.5 MHz			290	
		Frequency band: 0.5 to 1 MHz			650	

Table 7-14. PHY DPLL Electrical Characteristics (continued)

Parameter		Comments	Min	Typ	Max	Unit
Deterministic period jitter (input)					100	ps
Frequency error (input)					±150	ppm
Frequency error (output)					±500	ppm
Phase-to-phase variation					35	ps
Noise on digital 1.5-V supply					100	mV
Noise on analog 1.5-V supply					50	mV
Noise on analog 1.8-V supply					36	mV

7.2.4.10 PHY Power Consumption

Table 7-15 lists, by mode, the power consumption values of the modules.

Table 7-15. PHY Power Consumption

Supply	Min	Typ	Max	Unit
HS Mode				
VUSB.3P1		8.5		mA
VINTUSB1P8.OUT		25		mA
VINTUSB1P5.OUT		24		mA
VINTDIG.OUT		0.3		mA
FS Mode				
VUSB.3P1		13		mA
VINTUSB1P8.OUT		5.4		mA
VINTUSB1P5.OUT		17.5		mA
VINTDIG.OUT		0.3		mA
LS Mode				
VUSB.3P1		12.5		mA
VINTUSB1P8.OUT		5.4		mA
VINTUSB1P5.OUT		17.5		mA
VINTDIG.OUT		0.3		mA
Low-Power/Suspend Mode				
VUSB.3P1		0		mA
VINTUSB1P8.OUT		0		mA
VINTUSB1P5.OUT		2		μA
VINTDIG.OUT		0		mA
Power-Down Mode				
VUSB.3P1		0		mA
VINTUSB1P8.OUT		0		mA
VINTUSB1P5.OUT		2		μA
VINTDIG.OUT		0		mA

7.2.5 OTG Electrical Characteristics

The OTG block integrates three main functions:

- USB plug detection function on VBUS and ID
- ID resistor detection
- VBUS level detection

7.2.5.1 OTG VBUS Electrical

Table 7-16 lists the OTG VBUS electrical parameters.

Table 7-16. OTG VBUS Electrical

Parameter		Comments	Min	Typ	Max	Unit
VBUS Wake-Up Comparator						
VBUS wake-up delay	$DEL_{VBUS_WK_UP}$				15	µs
VBUS wake-up threshold	$V_{VBUS_WK_UP}$		0.5	0.6	0.7	V
VBUS Comparators						
A-device session valid	$V_{A_SESS_VLD}$		0.8	1.1	1.4	V
A-device V_{BUS} valid	$V_{A_VBUS_VLD}$		4.4	4.5	4.6	V
B-device session end	$V_{B_SESS_END}$		0.2	0.5	0.8	V
B-device session valid	$V_{B_SESS_VLD}$		2.1	2.4	2.7	V
VBUS Line						
A-device V_{BUS} input impedance to ground	$R_{A_BUS_IN}$	SRP (V_{BUS} pulsing) capable A-device not driving V_{BUS}			100	kΩ
B-device V_{BUS} SRP pulldown	$R_{B_SRP_DWN}$	5.25 V/8 mA, pullup voltage = 3 V	0.656	10		kΩ
B-device V_{BUS} SRP pullup	$R_{B_SRP_UP}$	(5.25 V – 3 V)/8 mA, pullup voltage = 3 V	0.281	1	2	kΩ
B-device V_{BUS} SRP rise time maximum for OTG-A communication	$t_{Rise_SRP_UP_Max}$	0 to 2.1 V with < 13 µF load			36	ms
B-device V_{BUS} SRP rise time minimum for standard host connection	$t_{Rise_SRP_UP_Min}$	0.8 to 2.0 V with > 97 µF load	60			ms
VBUS line maximum voltage		If VBUS_CHRG bit is low*			7	V

7.2.5.2 OTG ID Electrical

Table 7-17 lists the OTG ID electrical parameters.

Table 7-17. OTG ID Electrical

Parameter		Comments	Min	Typ	Max	Unit
ID Wake-Up Comparator						
ID wake-up comparator	$R_{ID_WK_UP}$	Wake up when ID shorted to ground through a resistor lower than 445 kΩ (±1%)	445			kΩ
ID Comparators—ID External Resistor Specifications						
ID ground comparator	R_{ID_GND}	ID_GND interrupt when ID shorted to ground through a resistor lower than 10 Ω	0	5	10	Ω
ID 100k comparators	R_{ID_100K}	ID_100K interrupt when 102 kΩ (1%) resistor plugged in	101	102	103	kΩ
ID 200k comparators	R_{ID_200K}	ID_200K interrupt when 200 kΩ (1%) resistor plugged in	198	200	202	kΩ
ID 440k comparators	R_{ID_440K}	ID_440K interrupt when 440 kΩ (1%) resistor plugged in	435	440	445	kΩ
ID float comparator	R_{ID_FLOAT}	ID_FLOAT interrupt when ID shorted to ground through a resistor higher than 560 kΩ	1400			kΩ
ID Line						
Phone I_D pullup to $V_{PH_ID_UP}$	$R_{PH_ID_UP}$	ID unloaded (VRUSB)	70	200	286	kΩ
Phone I_D pullup voltage	VPH_ID_UP	Connected to VRUSB	2.5		3.2	V
ID line maximum voltage					5.25	V

8 Battery Interface

8.1 General Description

8.1.1 Battery Charger Interface Overview

The TPS65950 has a BCI for complete battery management. The main function of the BCI is to control the charging of either 1-cell Li-ion or Li-ion polymer batteries, or 1-cell Li-ion batteries with cobalt-nickel-manganese anodes. It supports regulated ac chargers of 7-V absolute maximum and can charge with USB host devices, MCPC devices, USB chargers, or carkits of 7-V absolute maximum. The BCI can perform software-controlled linear charging with the sources mentioned, software-controlled pulsed charging with current-limited ac chargers, and automatic linear charging with ac chargers, USB chargers, and carkits.

The battery is monitored using the 10-bit ADC from the MADC to measure battery voltage, battery temperature, battery type, battery charge current, USB device input voltage, and ac charger input voltage. The magnitude of the charging current and the charging voltage is set by 10 bits of a programming register converted by a 10-bit DAC, whose output sets the reference input of the charging current and charging voltage control loop.

The BCI also performs monitoring functions:

- ac charger detection
- VBUS detection
- Battery detection
- ac charger overvoltage detection
- VBUS overvoltage detection
- Battery overvoltage detection
- Battery voltage level detection
- Battery charge current level detection
- Battery temperature out-of-range detection
- Battery end-of-charge detection
- Battery overcurrent detection
- Watchdog

8.1.2 Battery Backup Overview

The TPS65950 implements a backup mode, in which the backup battery keeps the RTC running. A rechargeable backup battery can be recharged from the main battery.

When the main battery is below 2.7 V or is removed, the backup battery powers the backup if the backup battery voltage is greater than 1.8 V. The backup domain powers up the following:

- Internal 32.768-kHz oscillator
- RTC
- Hash table (20 registers of 8 bits each)
- Eight GP storage registers

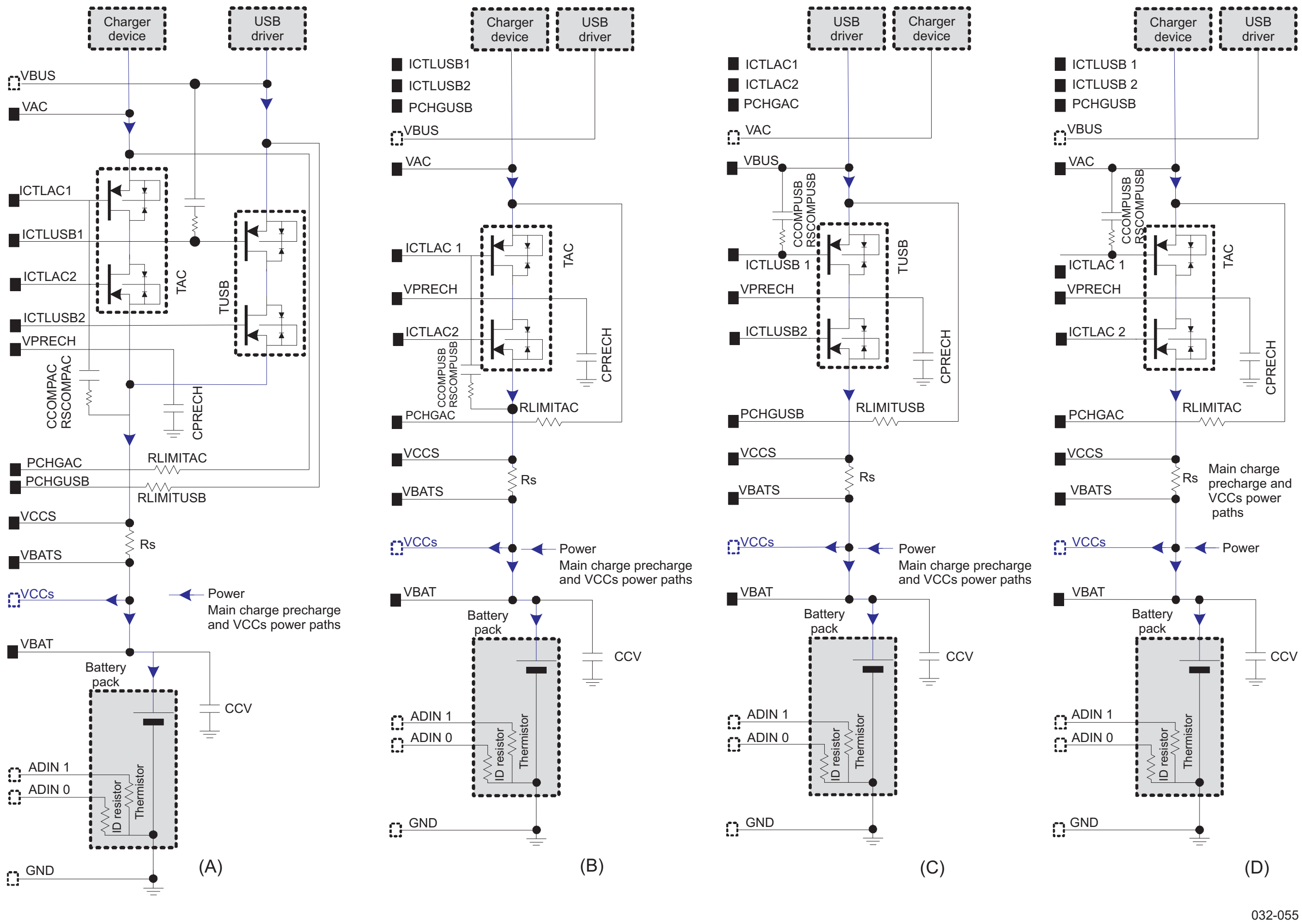
8.2 Typical Application Schematics

8.2.1 Functional Configurations

The BCI can be used in different configurations (see Figure 8-1). Each configuration requires a dedicated typical application schematic:

- ac charge supported (see Figure 8-1A, Figure 8-1B, and Figure 8-1D)
- USB charge supported (see Figure 8-1A and Figure 8-1C)

- ac constant voltage mode supported (see Figure 8-1A and Figure 8-1B)
- ac charger with current nonlimited (see Figure 8-1D)



A. Schematic that supports ac charge, ac constant voltage mode, and USB charge. With this ac compensation schematic, constant voltage mode is possible, but only current limited chargers are supported.
B. Schematic that supports only ac charge and ac constant voltage mode. With this ac compensation schematic, constant voltage mode is possible, but only current limited chargers are supported.
C. Schematic that supports only USB charge.
D. Schematic that supports only ac charge. With this ac compensation schematic, constant voltage mode is not possible, but current nonlimited chargers are supported.

Figure 8-1. Typical Application Schematics

NOTE

For the component values, see Table 15-1.

8.2.2 *In-Rush Current Limitation Schematic*

With the typical application schematic supporting constant voltage mode (Figure 8-1 A and B), battery in-rush current is limited by the charging device. The application schematic can be enhanced to support in-rush current at the charging device plug to maximum 850 mA as detailed by Figure 8-2. T3, R3, and C3 are connected between VAC and ICTLAC1 and intentionally bring in-rush cucation. The described enhancement is not required for Figure 8-1 D, where constant voltage mode is not supported.

Figure 8-2 shows a typical application schematic with in-rush current limitation.

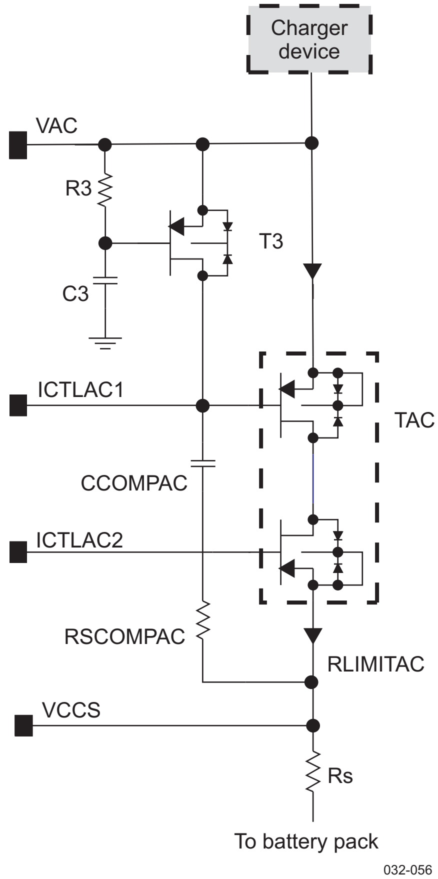


Figure 8-2. Typical Application Schematic (In-Rush Current Limitation)

8.2.3 Configuration With BCI Not Used

Figure 8-3 shows how to connect the BCI when it is not in use. The SUSPENDM bit must be set to disable the BCI internally.

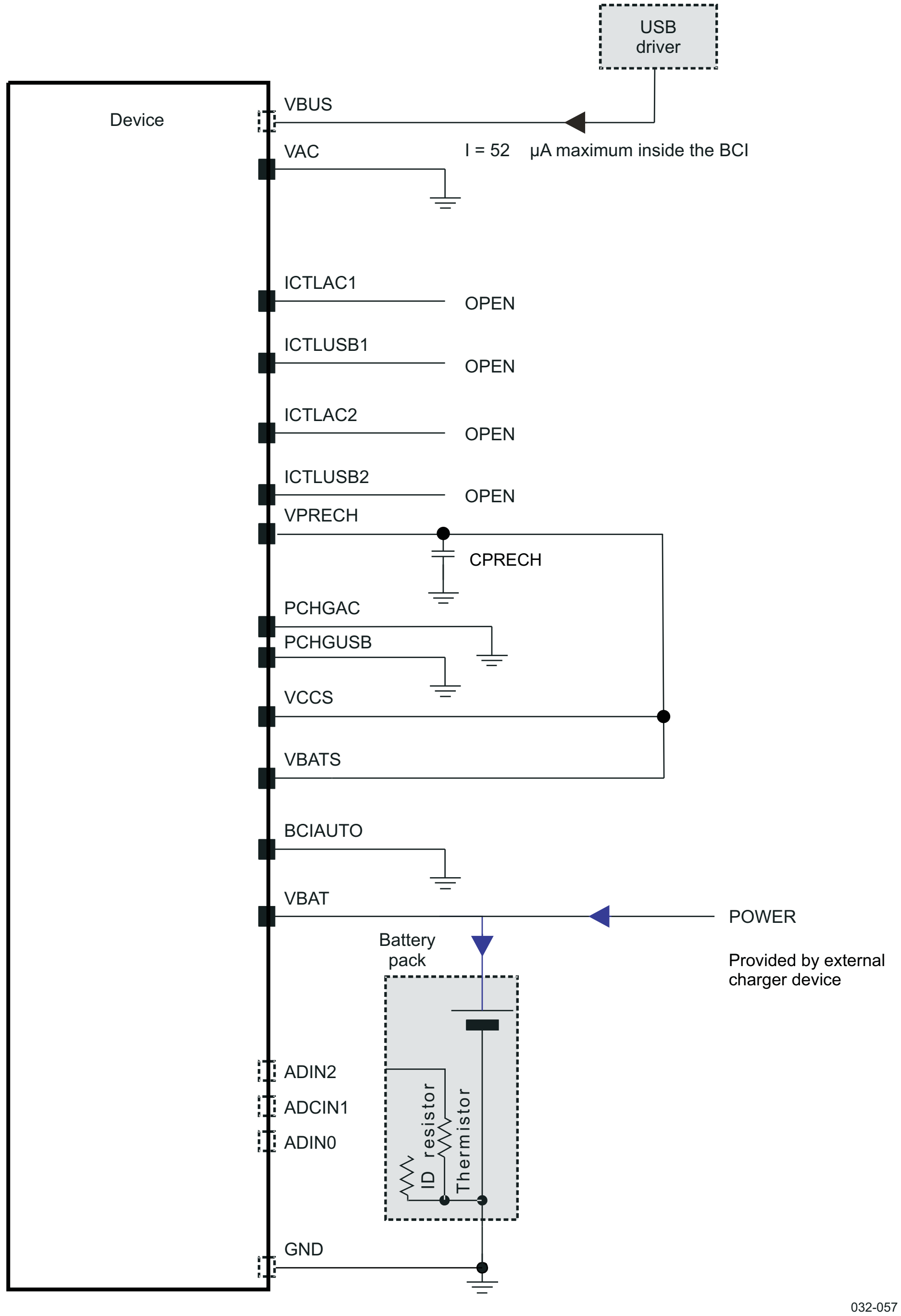


Figure 8-3. Typical Application Schematic (BCI Not Used)

8.3 Electrical Characteristics

This section describes the electrical characteristics of the BCI in the TPS65950.

8.3.1 Main Charge

Table 8-1 lists the electrical characteristics of the main charge.

Table 8-1. Main Charge Electrical Characteristics
VBAT = 3.6 V, R_S = 0.22 Ω, unless otherwise specified

Parameter	Test Conditions	Min	Typ	Max	Unit
VAC input voltage range[1]	dc voltage	4.8	5.4	7	V
VBUS input voltage range (external)	dc voltage	4.4	5	7	V
Charge current range				1.7	A
VAC accessory supply mode consumption	VBAT = 3.6 V, consumption on VBAT when ACCSUPEN = 1 and ACPATHEN = 1 connected to VBAT, current limitation enabled		0.75	1	mA
	VBAT = 3.6 V, consumption on VBAT when ACCSUPEN = 1 and ACPATHEN = 1 connected to VBAT, current limitation disabled		0.525	0.7	
VBUS accessory supply mode consumption	VBAT = 3.6 V, consumption on VBAT when ACCSUPEN = 1 and USBPATHEN = 1 connected to VBAT, current limitation enabled		0.64	0.85	mA
	VBAT = 3.6 V, consumption on VBAT when ACCSUPEN = 1 and USBPATHEN = 1 connected to VBAT, current limitation disabled		0.415	0.55	
ICTLAC1 output voltage swing (PWM charge)	$I_{ICTLAC1}$ = –10 μA, ACPATHEN = 1, PWMEN = 1, PWMDTYCY = 0x000	VAC–0.3			V
	$I_{ICTLAC1}$ = 10 μA, ACPATHEN = 1, PWMEN = 1, PWMDTYCY = 0x3FF			0.35	
ICTLAC1 output voltage swing (linear charge)	$I_{ICTLAC1}$ = –10 μA, ACPATHEN = 1, LINCHEN = 1, MESBAT = 1, CHGVREG = 0x000	VAC–0.3			V
	$I_{ICTLAC1}$ = 10 μA, ACPATHEN = 1, LINCHEN = 1, MESBAT = 1, CHGVREG = 0x3FF			0.35	
ICTLUSB1 output voltage swing (linear charge)	$I_{ICTLUSB1}$ = –10 μA, USBPATHEN = 1, LINCHEN = 1, MESBAT = 1, CHGVREG = 0x000	VBUS–0.3			V
	$I_{ICTLUSB1}$ = 10 μA, USBPATHEN = 1, LINCHEN = 1, MESBAT = 1, CHGVREG = 0x3FF			0.35	
ICTLAC2 output voltage swing (linear charge)	$I_{ICTLAC2}$ = –10 μA, ACPATHEN = 1, LINCHEN = 1, ACPATHEN = 0	VCCS–0.3			V
	$I_{ICTLAC2}$ = 10 μA, ACPATHEN = 1, LINCHEN = 1, ACPATHEN = 1			0.35	
ICTLUSB2 output voltage swing (linear charge)	$I_{ICTLUSB2}$ = –10 μA, USBPATHEN = 1, LINCHEN = 1, USBPATHEN = 0	VCCS–0.3			V
	$I_{ICTLUSB2}$ = 10 μA, USBPATHEN = 1, LINCHEN = 1, USBPATHEN = 1			0.35	
PWM mode output current	PWM = 1 (ICTLAC1 = 0), VAC = 6.8 V		5.0		mA
	PWM = 0 (ICTLAC1 = VAC), VAC = 6.8 V		–2.0		

(1) The maximum voltage value of the charging device is 7 V (process limitation). The minimum voltage value of the charging device is: VBATMAX + 2 PMOS drop + 0.22 Ω resistor drop
(where VBATMAX is the maximum voltage value of the battery; that is, 4.2 V for Li-ion battery)
User must consider maximum dissipation while using maximum ac/USB voltage (7 V) or maximum current load (1.7 A).

Table 8-1. Main Charge Electrical Characteristics VBAT = 3.6 V, R_S = 0.22 Ω, unless otherwise specified (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
ac main charge battery removal switch-off time	CHGIREG = (value relative to I_{CHG} = 0.6 A), VAC = 5.4 V, C = 100 nF connected to ICTLAC1, VBAT threshold = 4.55 V, measure charge current from removal to 10% Miller compensation			150	µs
	CHGIREG = (value relative to I_{CHG} = 0.6 A), VAC = 5.4 V, C = 100 nF connected to ICTLAC1, VBAT threshold = 4.55 V, measure charge current from removal to 10% Regular compensation			150	
USB main charge battery removal switch-off time	CHGIREG = (value relative to I_{CHG} = 0.6 A), VBUS = 5.0 V, C = 100 nF connected to ICTLUSB1, VBAT threshold = 4.55 V, measure charge current from removal to 10%			150	µs
VAC-to-MADC input attenuation	VAC from 4.8 V to 6.8 V (maximum MADC input voltage = 1.224 V)	0.12	0.15	0.18	V/V
VBAT-to-MADC input attenuation	VBAT from 3.0 V to 4.5 V (maximum MADC input voltage = 1.35 V)	0.2	0.25	0.3	V/V
Current-to-voltage conversion slope(2)	(VCCS–VBATS) rising from 0 V to 0.17 V: CGAIN = 0 equivalent to 0–775 mA range	0.704	0.88	1.056	mV/mA
	(VCCS–VBATS) rising from 0 V to 0.33 V: CGAIN = 1 equivalent to 0–1500 mA range	0.352	0.44	0.528	
Current-to-voltage conversion positive offset	OFFSEN = 1, OFFSN[1:0] = 00, CGAIN = 0, OFFSIGN = 0		18.7		mV
	OFFSEN = 1, OFFSN[1:0] = 01, CGAIN = 0, OFFSIGN = 0		38.8		
	OFFSEN = 1, OFFSN[1:0] = 10, CGAIN = 0, OFFSIGN = 0		60.1		
	OFFSEN = 1, OFFSN[1:0] = 11, CGAIN = 0, OFFSIGN = 0		82.6		
Current-to-voltage conversion negative offset	OFFSEN = 1, OFFSN[1:0] = 00, CGAIN = 0, OFFSIGN = 1		–18.2		mV
	OFFSEN = 1, OFFSN[1:0] = 01, CGAIN = 0, OFFSIGN = 1		–35.6		
	OFFSEN = 1, OFFSN[1:0] = 10, CGAIN = 0, OFFSIGN = 1		–52.2		
	OFFSEN = 1, OFFSN[1:0] = 11, CGAIN = 0, OFFSIGN = 1		–67.6		
Charge voltage and charge current DAC	Linear range	1FF		3BA	hex
	Differential nonlinearity	–2		2	LSB
	Integrated nonlinearity	–2		2	LSB
	Offset	–25		25	mV
ADIN0 dc current source	ADIN0 = 1 V	7	10	13	µA
ADCIN1 dc current source	ADCIN1 = 1 V, ITHSENS[2:0] = 000 (maximum MADC input voltage = 0.875 V), After TRIM done by ISRCTRIM[3:0], at ambient temperature	9.875	10	10.125	µA

(2) MADC output code = (VCCS – VBATS) × 4 with CGAIN = 0
MADC output code = (VCCS – VBATS) × 2 with CGAIN = 1

Table 8-1. Main Charge Electrical Characteristics VBAT = 3.6 V, R_S = 0.22 Ω, unless otherwise specified (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
ADCIN1 dc current source for temperature measurement	ADCIN1 = 1 V, ITHSENS[2:0] = 000 (maximum MADC input voltage = 0.875 V), after TRIM done by ISRCTRIM[3:0]	9.5	10	10.5	μA
	ITHSENS[2:0] = 001	14	20	26	
	ITHSENS[2:0] = 010	21	30	39	
	ITHSENS[2:0] = 011	28	40	52	
	ITHSENS[2:0] = 100	35	50	65	
	ITHSENS[2:0] = 101	42	60	78	
	ITHSENS[2:0] = 110	49	70	91	
	ITHSENS[2:0] = 111	56	80	104	
Constant current loop accuracy	After trimming (±1.10%), VAC = 5.4 V or VBUS = 5.0 V, VBAT = 3.6 V, CHGIREG = (value relative to I_{CHG} = 0.6 A), VCCS–VBATS rising voltage, monitoring ICTLAC1 or ICTLUSB1, CGAIN = 1, overtemperature (ambient 0°C to 50°C) (including the bandgap accuracy overtemperature ±0.5% and the R_{sense} resistor accuracy ±1%)	–11%		11%	
	After trimming (±0.55%), VAC = 5.4 V or VBUS = 5.0 V, VBAT = 3.6 V, CHGIREG = (value relative to I_{CHG} = 0.6 A), VCCS–VBATS rising voltage, monitoring ICTLAC1 or ICTLUSB1, CGAIN = 0, overtemperature (ambient 0°C to 50°C) (including the bandgap accuracy overtemperature ±0.5% and the R_{sense} resistor accuracy ±1%)	–3.15%		3.15%	
Constant current loop offset	At error amplifier input, before loop trim. Including DAC offset, I-to-V offset after I-to-V trim, error amplifier offset	–46.8		46.8	mV
Constant voltage loop accuracy	After trimming (±0.14%), VAC = 5.4 V or VBUS = 5.0 V, at room temperature, CHGVREG = (value relative to VBAT = 4.37 V), VBAT rising voltage, monitoring ICTLAC1 or ICTLUSB1	–0.28%		0.28%	
	After trimming (±0.14%), VAC = 5.4 V or VBUS = 5.0 V overtemperature (ambient 0°C to 50°C), CHGVREG = (value relative to VBAT = 4.37 V), VBAT rising voltage, monitoring ICTLAC1 or ICTLUSB1 (including the bandgap accuracy overtemperature ±0.5%)	–0.82%		0.82%	
Charger presence detect threshold	VBAT = 3.6 V, rising edge	VBAT+0.3	VBAT+0.4	VBAT+0.6	V
	VBAT = 3.6 V, falling edge	VBAT	VBAT+0.1	VBAT+0.3	
Battery threshold when default value(3)	VAC = 5.4 V or VBUS = 5.0 V, VBATOVEN = 1, VBATOVTH(3:0) = default, MESBAT = 1, VBAT rising voltage, monitoring VBATOV status signal	4.45	4.55	4.65	V
ac charger overvoltage threshold when default value(3)	VBAT = 3.6 V, VACCHGOVEN = 1, VACCHGOVTH(3:0) = default, VAC rising voltage, monitoring VACCHGOV status signal	6.24	6.5	7	V
VBUS overvoltage threshold when default value(3)	VBAT = 3.6 V, VBUSOVEN = 1, VBUSOVTH(3:0) = default, VBUS rising voltage, monitoring VBUSOV status signal	5.28	5.5	5.9	V
Main charge main battery presence impedance detection threshold	Measured through ADCIN1 rising voltage and sourced current, monitoring BATSTS value	67.5	75	82.5	kΩ
Main charge main battery presence voltage detection threshold	Force ADCIN1 voltage, monitor BATSTS value		750		mV
Temperature detection accuracy	For low temperature (2°C/3°C) For high temperature (43°C/50°C)	–3 –5		3 5	°C
Battery voltage accuracy	Tested for VBAT = 2.9, 3.6, and 4.2 V	VBAT–0.1	VBAT	VBAT+0.1	V
Current charge accuracy	Tested for ICHG = 600 mA	ICHG–0.04	ICHG	ICHG+0.04	A

(3) Can be changed by programming the associated threshold register

Table 8-1. Main Charge Electrical Characteristics
VBAT = 3.6 V, R_S = 0.22 Ω, unless otherwise specified (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Battery Rs	ESR (including FUSE)			0.5	Ω

8.3.2 Precharge

During slow precharge and fast precharge, a precharge voltage loop is always enabled and limits the battery voltage charge to 3.6 V typical. To use the constant voltage loop, a battery voltage prescaler is also always enabled. The voltage loop is nonlinear. A fast comparator switches off the external power portable media operating system (PMOS) when VBAT is higher than 3.6 V and switches on the PMOS when VBAT is lower than 3.6 V. When the USB charger is used, fast precharge is not available (to comply with USB standards).

In precharge mode, the threshold of the ac charger overvoltage detection is forced to 6.8 V.

Table 8-2 lists the precharge electrical characteristics.

Table 8-2. Precharge Electrical Characteristics
R_S = 0.22 Ω, unless otherwise specified

Parameter	Test Conditions	Min	Typ	Max	Unit
ICTLAC1 output voltage swing (precharge)	$I_{ICTLAC1}$ = –10 μA, VBAT = 1.5 V, VCCS = VBAT+200 mV, VAC = 5.4 V, SYSACTIV = 0	VAC–0.3			V
	$I_{ICTLAC1}$ = 10 μA, VBAT = 1.5 V, VCCS = VBAT, VAC = 5.4 V, SYSACTIV = 0			0.35	
ICTLUSB1 output voltage swing (precharge)	$I_{ICTLUSB1}$ = –10 μA, VBAT = 1.5 V, VCCS = VBAT+200 mV, VAC = 0.0 V, VBUS = 5 V, SYSACTIV = 0	VAC–0.3			V
	$I_{ICTLUSB1}$ = 10 μA, VBAT = 1.5 V, VCCS = VBAT, VAC = 0.0 V, VBUS = 5 V, SYSACTIV = 0			0.35	
ICTLAC2 output voltage swing (precharge)	$I_{ICTLAC2}$ = –10 μA, VBAT = 1.5 V, VCCS = VBAT+200 mV, VAC = 5.4 V, SYSACTIV = 0	VCCS–0.3			V
	$I_{ICTLAC2}$ = 10 μA, VBAT = 1.5 V, VCCS = VBAT, VAC = 5.4 V, SYSACTIV = 0			0.35	
ICTLUSB2 output voltage swing (precharge)	$I_{ICTLUSB2}$ = –10 μA, VBAT = 1.5 V, VCCS = VBAT+200 mV, VAC = 0.0 V, VBUS = 5 V, SYSACTIV = 0	VCCS–0.3			V
	$I_{ICTLUSB2}$ = 10 μA, VBAT = 1.5 V, VCCS = VBAT, VAC = 0.0 V, VBUS = 5 V, SYSACTIV = 0			0.35	
ac precharge battery removal switch-off time	In fast precharge, Rlimit = 700 kΩ, VAC = 5.4 V, VBAT threshold = 3.6 V, measure charge current from removal to 10%			150	μs
USB precharge battery removal switch-off time	In precharge, Rlimit = 500 kΩ, VBUS = 5.0 V, VBAT threshold = 3.6 V, measure charge current from removal to 10%			150	μs
PCHGPOR voltage threshold	VAC = 5.4 V or VBUS = 5.0 V, PCHGPOR raise when VPRECH voltage higher than the voltage threshold		1.2		V
PCHGCLK click frequency	VAC = 5.4 V or VBUS = 5.0 V (including temperature variation)	18.5	32	45.4	kHz
	VAC = 5.4 V or VBUS = 5.0 V (at room temperature)	24.3	32	39.68	
PCHGVREF band gap voltage	VAC = 5.4 V or VBUS = 5.0 V	0.7125	0.75	0.7875	V
VPRECH regulator output	VAC = 5.4 V or VBUS = 5.0 V	1.4	1.5	1.6	V
Small precharge output current	VBAT = 0.0 V, VAC = 5.4 V or (VBUS = 5.0 V and USBSLOWPCHG = 1)	3	5	7	mA
Slow precharge loop accuracy	After TRIMinG, VAC = 5.4 V or VBUS = 5.0 V, VBAT = 1.5 V, VCCS–VBATS rising voltage, monitoring ICTLAC1 or ICTLUSB1	14	17.2	20.3	mV

Table 8-2. Precharge Electrical Characteristics
R_S = 0.22 Ω, unless otherwise specified (continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Fast precharge loop accuracy	After TRIMinG, PCHGAC or PCHGUSB floating, VAC = 5.4 V, VBAT = 3.0 V, VCCS–VBATS rising voltage, monitoring ICTLAC1 or ICTLUSB1	56	68.8	81.2	mV
Precharge constant voltage loop limitation	System did not start after VBAT > 3.2 V, VBATS input.	3.4	3.6	3.8	V
VBUSOVPRECH threshold (for USB reliability)	VBUS input	5.04	5.25	5.46	V
ac charger overvoltage threshold	VBAT = 2.8 V, VAC input	6.5	6.8	7.3	V
VBUS overvoltage threshold	VBAT = 2.8 V, VBUS input	6.5	6.8	7.3	V
Battery voltage threshold to start ac fast precharge	VBATS input	1.8	2.0	2.2	V
Battery voltage threshold to start ac slow precharge	VBATS input	1.0	1.2	1.4	V
Charger presence detect threshold	VBATS = 2.8 V, rising edge	VBAT+0.3	VBAT+ 0.4	VBAT+0.6	V
	VBATS = 2.8 V, falling edge	VBAT	VBAT+ 0.1	VBAT+0.3	
VBUS presence detect threshold	Rising edge			4.4	V
	Falling edge			4.3	
BCIAUTO detection impedance threshold	To obtain CVENACA = BCIAUTOACA = 0			10	kΩ
	To obtain CVENACA = BCIAUTOACA = 1	140			
BCIAUTO detection voltage threshold	CVENACA = 0 below the voltage threshold	100	150	200	mV
	CVENACA = 1 below the voltage threshold	700	750	800	
BCIAUTO detection output current	Measured on BCIAUTO pin	4.5	7.5	9.5	μA
Precharge main battery presence impedance detection threshold	Measured through ADCIN1 rising voltage and sourced current, monitoring BATSTS value	115	140	192	kΩ
Precharge main battery presence voltage detection threshold	Force ADCIN1 voltage, monitor BATSTS value.		750		mV
Precharge main battery presence detection output current	Measured on ADCIN1 pin		5.5		μA

8.3.3 Constant Voltage Mode

The BCI supports a constant voltage (CV) mode. CV mode is automatically started when there is no battery pack, a regulated ac charger is plugged in, and CVENAC = 1. The charging device outputs a constant voltage at the VBAT node. To start CV mode, the precharge analog hardware detects whether a battery pack is open using the battery presence comparator, and detects whether an ac charger is connected using the ac charger presence comparator.

CV mode is disabled when VAC is greater than 6.5 V typical. ac overvoltage protection is also enabled during CV mode.

Hardware implementation for CV mode uses the main charge constant voltage loop. In CV mode, a 35-mA typical load is synced internally to keep the regulated VBAT voltage output stable. An 80-μF typical external capacitor must be connected to the VBAT node.

Table 8-3 lists the electrical characteristics of CV mode.

Table 8-3. CV Mode Electrical Characteristics(1)

Parameter	Test Conditions	Min	Typ	Max	Unit
Main charge constant voltage mode	VAC = 5.4 V, ADCIN1 pin floating, LDOOK = 1				
CBAT	Battery node capacitor	37	80	167	μF
	ESR (including FUSE)		0.4	0.5	Ω
VBAT regulated voltage, including dc (posttrim), dc load regulation, and dc line regulation	Typical condition is VBAT for VAC = 5.4 V, ILOAD = 0.5 A	3.88	4.0	4.12	V
	dc load regulation: VAC = VACmin, ILOAD varying from 0 to ILOADmax				
	dc line regulation: ILOAD = ILOADmax, VAC varying from VACmin to VACmax				
	Maximum condition is ILOAD = 0, VAC = 6.2 V				
	Minimum condition is ILOAD = 1 A, VAC = 4.8 V				
ILOAD				1	A
BCI VBAT load current	VAC = 5.4 V	15	35	55	mA
VAC		4.8	5.4	6.2	V
Transient load regulation during internal LDO startup	VBAT(Iout 20 mA) – VBAT(Iout 500 mA) in load change time = 1 μs (BCI in precharge CV mode)	300		300	mV
Transient load during LDO and dc-dc startup	VBAT(Iout 30 mA) – VBAT(Iout 830 mA) in load change time = 1 μs (BCI in main charge CV mode)	300		300	mV
Transient load regulation	VBAT(Iout 30 mA) – VBAT(Iout 300 mA) in load change time = 1 μs (BCI in main charge CV mode) (ESR = 0.4 Ω)	100		100	mV

(1) In CV mode, an external FET characteristic is critical. This mode has been validated for FDJ1027P FET.

8.4 Charge Sequence Timing Diagram

Figure 8-4 is the charge sequence timing diagram.

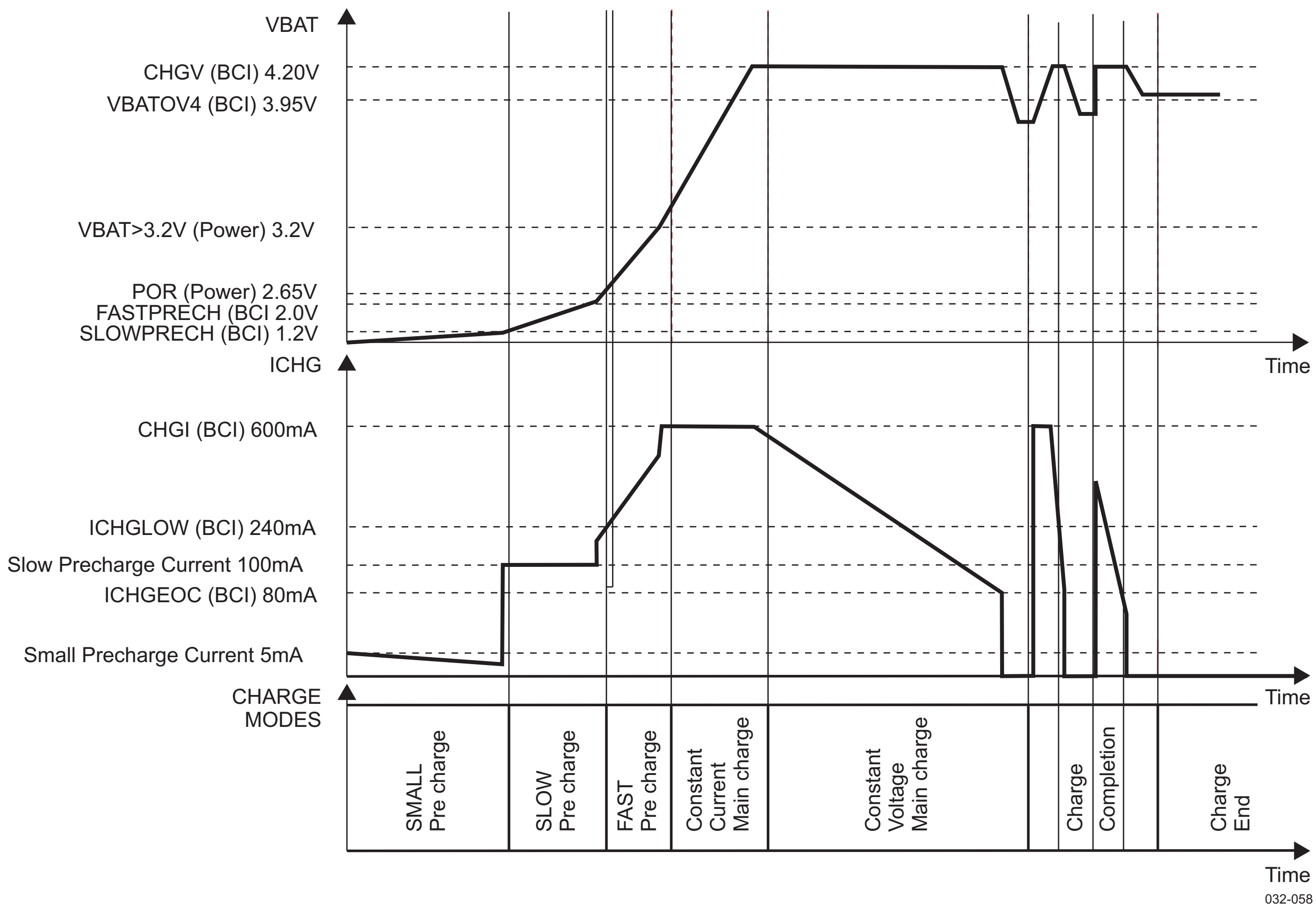


Figure 8-4. Automatic Charge Sequence Timing Diagram

8.5 CEA Charger Type

Depending on the device and according to the charger type, the DM and DP lines have different characteristics:

- Hub: DP and DM not shorted, DM low
- Charger: DP and DM shorted
- Carkit: DP and DM not shorted, DM high

These characteristics reflect to which of these devices the phone is connected.

Table 8-4 lists the important characteristics in precharge detection.

Table 8-4. Precharge Detection Characteristics

Symbol	Parameter	Comments	Min	Max	Unit
I_{CCINIT}	Supply current of unconfigured function/hub	Hub: DP and DM not shorted, DM low		100	mA
I_{CRINIT}	Supply current of unconfigured charger/carkit	Charger: DP and DM shorted Carkit: DP and DM not shorted, DM high		100	mA
T_{DELAY}	Delay for power up all blocks		1000		μs
T_{DMOD_DELAY}	Time pulling down DM line		19.5		μs

Table 8-4. Precharge Detection Characteristics (continued)

Symbol	Parameter	Comments	Min	Max	Unit
T_{CHECK}	Repeat time check process			500	ms
T_{PULSE}	DP pullup pulse width			20	ms

In main charge, the basic chargers and basic carkits indicate their default current limit, versus the value of the ID resistor, between the ID pin and the ground, and also versus the data bus D± connection type (shorted or not shorted).

Table 8-5 lists the output current limit ranges according to the device type and parameters.

Table 8-5. Main Charge Current Limit Indication

Device Type	Parameter					Output Current Limit		
	ID Resistor (1%)	Output Voltage (nom)	D+/D– Connection (1)	ID Pin State	ID Pin Current Limit Implemented	Min	Max	Unit
Phone-powered accessory	102k	N/A (2)	Not shorted	N/A	N/A	N/A	N/A	
Charger 5-wire	200k	5.0 V	Shorted	Low	N/A	450	650	mA
				High	No	450	650	
				High	Yes	750	950	
	440k	5.0 V	Shorted	Low	N/A	750	950	mA
				High	No	750	950	
		4.5 V	Shorted	High	Yes	1.8	3.0 (3)	A
Basic carkit 5-wire	200k	5.0 V	D-high	Used for muting	N/A	450	650	mA
	440k	5.0 V	D-high	Used for muting	N/A	750	950	
Smart carkit 5-wire	N/A	5.0 V	D-high	N/A	N/A	0.450	3.0 (3)	A
Carkit 4-wire	N/A	5.0 V	D-high	N/A	N/A	0.450	3.0 (3)	A

(1) Shorted indicates that D+ (DP) is shorted to D– (DM).
(2) N/A = Not applicable
(3) The maximum current limit in this configuration is for safety. It does not indicate normal current loads for the phone.

9 MADC

9.1 General Description

The TPS65950 shares the MADC resource with the host processors in the system (hardware and software conversion modes) and its BCI. Therefore, the TPS65950 must:

- Manage potential concurrent requests of conversions and priority among resource users
- Flag, using interrupt signals, the end-of-sequence of conversions
- Grant quarter-bit accuracy for modem conversion of battery voltage

The quarter-bit accurate start signal is provided through a STARTADC from the host processor (real-time conversion).

The MADC generates interrupt signals to the host processors. Interrupts are handled primarily by the MADC internal secondary interrupt handler (SIH) and secondly at the upper level (outside the MADC) by the TPS65950 primary interrupt handler (PIH). The MADC indicates to the BCI module, through a data ready signal, that conversion results are available.

9.2 Main Electrical Characteristics

Table 9-1 lists the electrical characteristics of the MADC.

Table 9-1. Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Resolution			10		Bit
Input dynamic range for external input	Except ADIN0 and ADCIN1 and internal MADC input (0 to 1.5 V)	0		2.5	V
MADC voltage reference			1.5		V
Differential nonlinearity	For all channels (except ADIN2 through ADIN7 channels)	–1		1	LSB
Integral nonlinearity	Best fitting. For all channels (except ADIN2 through ADIN7)	–2		2	LSB
Differential nonlinearity for ADIN2 through ADIN7		–1		1	LSB
Integral nonlinearity for ADIN2 through ADIN7	Best fitting for codes 230 to maximum	–2		2	LSB
	Best fitting considering offset of 25 least-significant bits (LSBs)	–3.75		3.75	LSB
Offset	Best fitting	–28.5		28.5	mV
Input bias			1		µA
Input capacitor C_{BANK}				10	pF
Maximum source input resistance Rs (for all 16 internal or external inputs)				100	kΩ
Input current leakage (for all 16 internal or external inputs)				1	µA

9.3 Channel Voltage Input Range

Table 9-2 lists the channel voltage input ranges.

Table 9-2. Analog Input Voltage Range

Channel	Min	Typ	Max	Unit	Prescaler
ADIN0: Battery type/GP input	0		1.5	V	No prescaler dc current source for battery identification through external resistor (10 μA typical)
ADCIN1: Battery temperature	0		1.5	V	No prescaler dc current source for temperature measurement through external resistor (10 to 80 μA programmable)
ADIN2: GP input(1)	0		2.5	V	MADC prescaler from 0 to >1.5 V
ADIN3: GP input(1)	0		2.5	V	MADC prescaler from 0 to >1.5 V
ADIN4: GP input(1)	0		2.5	V	MADC prescaler from 0 to >1.5 V
ADIN5: GP input(1)	0		2.5	V	MADC prescaler from 0 to >1.5 V
ADIN6: GP input(1)	0		2.5	V	MADC prescaler from 0 to >1.5 V
ADIN7: GP input(1)	0		2.5	V	MADC prescaler from 0 to >1.5 V

(1) GP inputs must be tied to ground when TPS65950 internal power supplies (VINTANA1 and VINTANA2) are off.

9.3.1 Sequence Conversion Time (Real-Time or Nonaborted Asynchronous)

Table 9-3 lists the sequence conversion timing characteristics. Figure 9-1 is a conversion sequence general timing diagram.

Table 9-3. Sequence Conversion Timing Characteristics

Parameter	Comments	Min	Typ	Max	Unit
F	Running frequency		1		MHz
T = 1/F	Clock period		1		μs
N	Number of analog inputs to convert in a single sequence	0		16	
Tstart	SW1, SW2, or USB asynchronous request or real-time STARTADC request	3		4	μs
Tsettling time	Settling time to wait before sampling a stable analog input (capacitor bank charge time) Tsettling is calculated from the max ((Rs + Ron)*Cbank) of the 16 possible input sources (internal or external). Ron is the resistance of the selection analog input switches (5 kΩ). This time is software-programmable in the open-core protocol (OCP) register.	5	12	20	μs
Tstartsar	The successive approximation registers ADC start time.		1		μs
Tadc time	The successive approximation registers ADC conversion time.		10		μs
Tcapture time	Tcapture time is the conversion result capture time.		2		μs
Tstop		1		2	μs
Full conversion sequence time	One channel (N = 1)(1)	22		39	μs
	All channels (N = 16)(1)	352		624	
Conversion sequence time	Without Tstart and Tstop: One channel (N = 1)(1)	18		33	μs
	Without Tstart and Tstop: All channels (N = 16)(1)	288		528	
STARTADC pulse duration	STARTADC period is T	0.33		24	μs

(1) Total sequence conversion time general formula: Tstart + N*(1 + Tsettling + Tadc + Tcapture) +Tstop

Table 9-3 shows the information in Figure 9-1. The *Busy* parameter shows that a conversion sequence is running, and the *channel N result register* parameter corresponds to the result register of RT/GP/BCI selected channel.

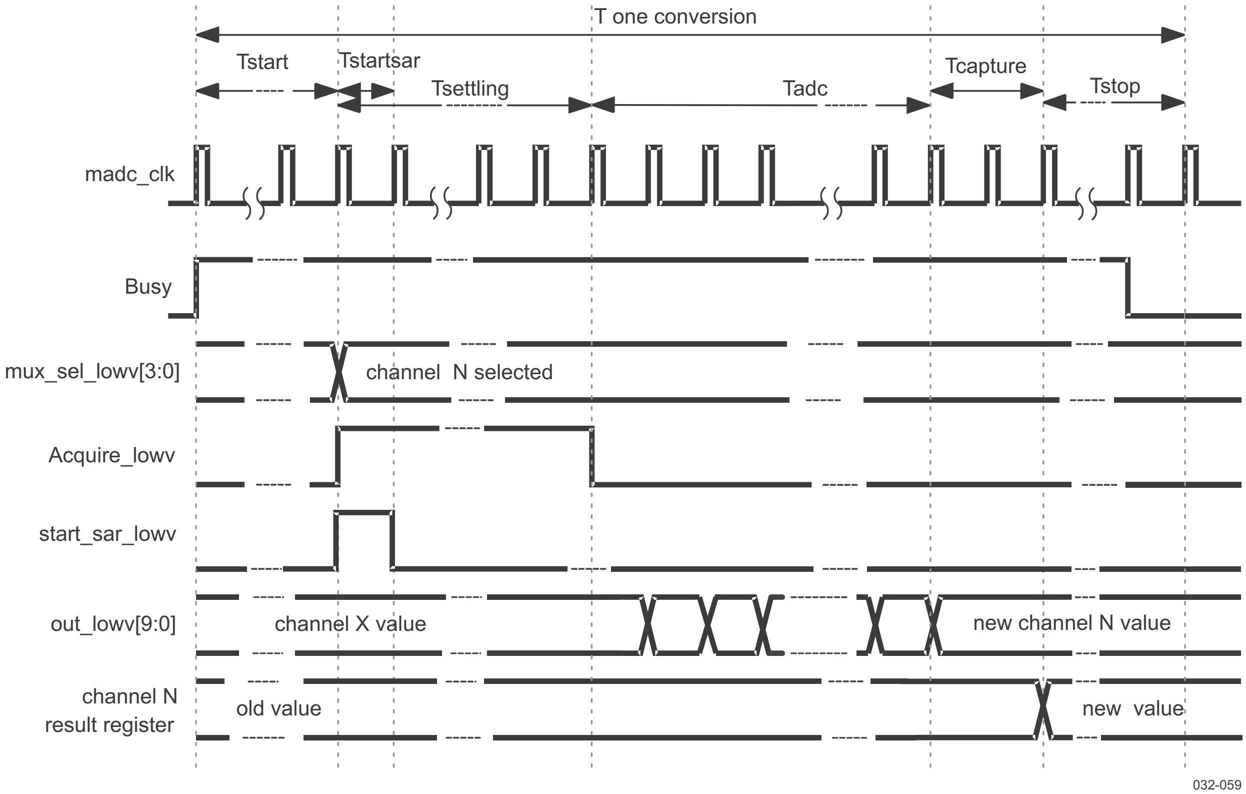


Figure 9-1. Conversion Sequence General Timing Diagram

10 LED Drivers

10.1 General Description

Two arrays of parallel LEDs are driven (dedicated for the phone light). The parallel LEDs are supplied by VBAT and the external resistor value is given for each of them. The TPS65950 has two open-drain LED drivers for keypad backlighting. The keypad backlighting must incorporate any required current limiting and be rated for operation at the main battery voltage.

Figure 10-1 is a block diagram of the LED driver. Table 10-1 lists the electrical characteristics of the LED driver.

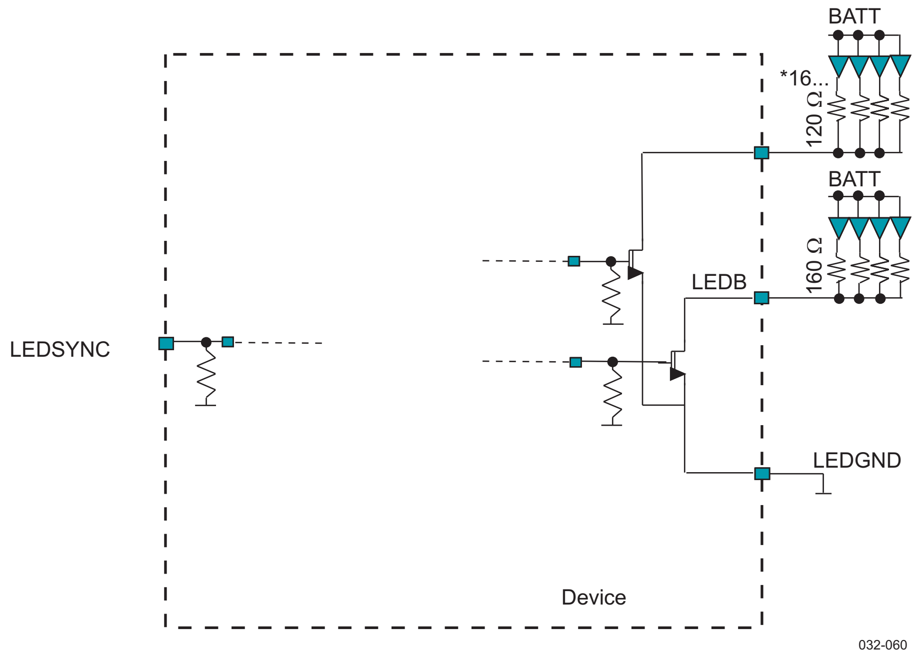


Figure 10-1. LED Driver Block Diagram

For the component values, see Table 15-1.

Table 10-1. Electrical Characteristics

Parameter	Conditions	Min	Typ	Max	Unit
Software On resistance	I_O = 160 mA		3	4	Ω
	I_O = 60 mA		10	12	

11 Keyboard

11.1 Keyboard Connection

The keyboard is connected to the chip using:

- KBR (7:0) input pins for row lines
- KBC (7:0) output pins for column lines

Figure 11-1 shows the keyboard connection.

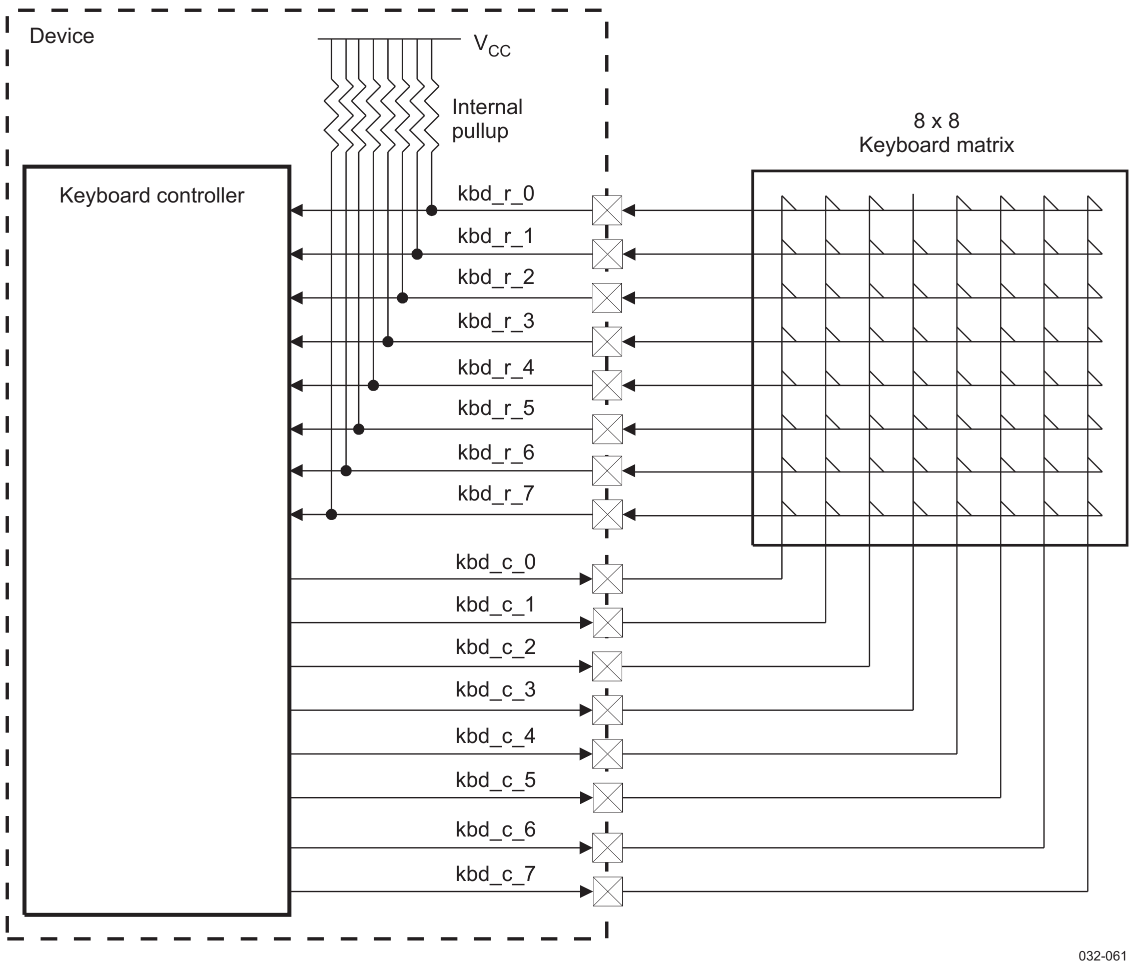


Figure 11-1. Keyboard Connection

When a key button of the keyboard matrix is pressed, the corresponding row and column lines are shorted together. To allow key press detection, all input pins (KBR) are pulled up to V_{CC} and all output pins (KBC) are driven low.

Any action on a button generates an interrupt to the sequencer.

The decoding sequence is written to allow detection of simultaneous press actions on several key buttons.

The keyboard interface can be used with a smaller keyboard area than 8 × 8. To use a 6 × 6 keyboard, KBR(6) and KBR(7) must be tied high to prevent any scanning process distribution.

12 Clock Specifications

The TPS65950 includes several I/O clock pins. The TPS65950 has two sources of high-stability clock signals: the external high-frequency clock (HFCLKIN) input and an onboard 32-kHz oscillator (an external 32-kHz signal can be provided). Figure 12-1 is an overview of the clocks.

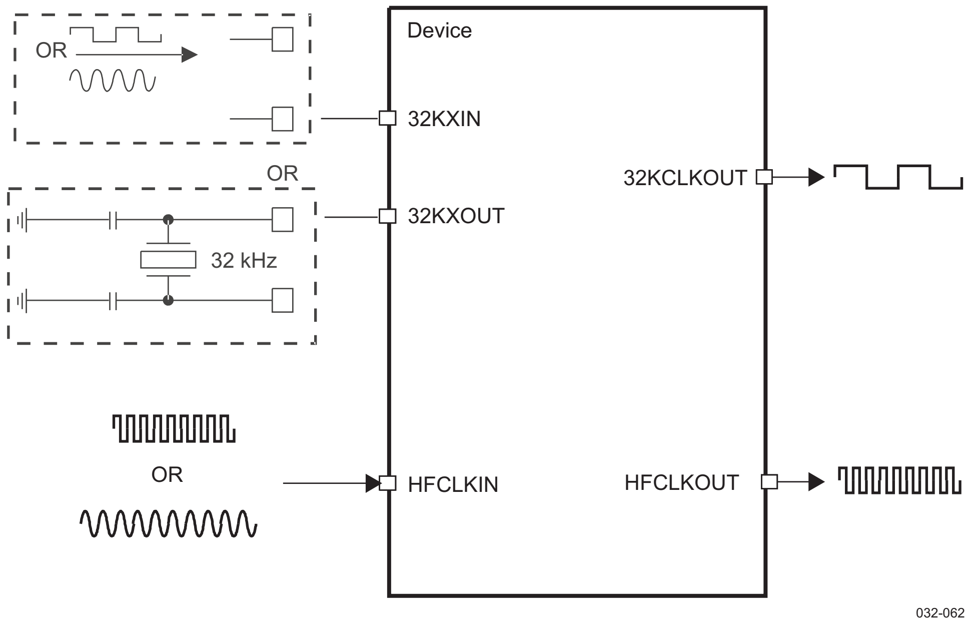


Figure 12-1. Clock Overview

12.1 Features

The TPS65950 accepts two sources of high-stability clock signals:

- 32KXIN/32KXOUT: Onboard 32-kHz crystal oscillator (an external 32-kHz input clock can be provided)
- HFCLKIN: External high-frequency clock (19.2, 26, or 38.4 MHz).

The TPS65950 can provide:

- 32KCLKOUT digital output clock
- HFCLKOUT digital output clock with the same frequency as the HFCLKIN input clock

12.2 Input Clock Specifications

The clock system accepts two input clock sources:

- 32-kHz crystal oscillator clock or sinusoidal/squared clock
- HFCLKIN high-frequency input clock

12.2.1 Clock Source Requirements

Table 12-1 lists the input clock requirements.

Table 12-1. TPS65950 Input Clock Source Requirements

Pad	Clock Frequency		Stability	Duty Cycle
32KXIN 32KXOUT	32.768 kHz	Crystal	±30 ppm	40%/60%
		Square wave	–	45%/55%
		Sine wave	–	–
HFCLKIN	19.2, 26, 38.4 MHz	Square wave	±150 ppm	See (1)
		Sine wave	–	–

(1) HFCLK duty cycle and frequency is not altered by the internal circuit. The input clock accuracy must match that of the system requirement, for example, OMAP device.

12.2.2 High-Frequency Input Clock

HFCLKIN is the high-frequency input clock. It can be a square- or sine-wave input clock. If a square-wave input clock is provided, it is recommended to switch the block to bypass mode when possible to avoid loading the clock.

Figure 12-2 shows the HFCLKIN clock distribution.

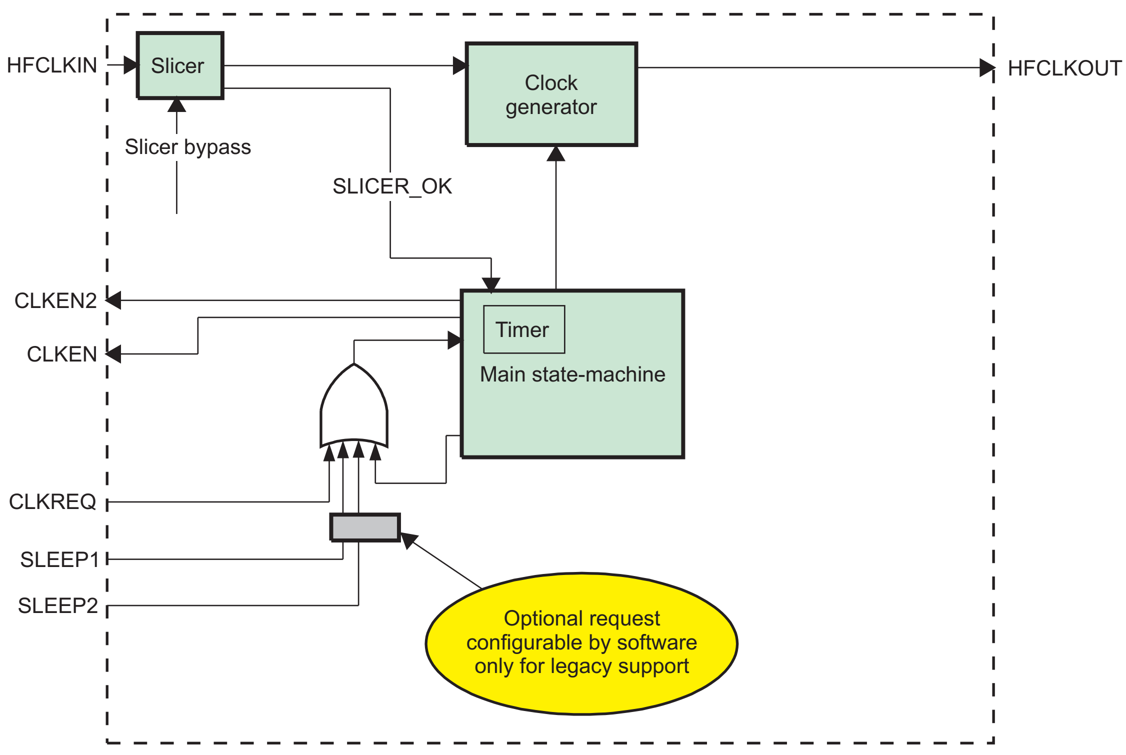


Figure 12-2. HFCLKIN Clock Distribution

When a device needs a clock signal other than 32.768 kHz, it makes a clock request and activates the CLKREQ pin. As a result, the TPS65950 immediately sets CLKEN to 1 to warn the clock provider in the system about the clock request and starts a timer (maximum of 5.2 ms using the 32.768-kHz clock). When the timer expires, the TPS65950 opens a gated clock, the timer automatically reloads the defined value, and a high-frequency output clock signal is available through the HFCLKOUT pin. The output drive of HFCLKOUT is programmable (minimum load 10 pF, maximum load 40 pF) and must be at 40 pF by default.

With a register setting, the mirroring of CLKEN can be enabled on CLKEN2. When this mirroring feature is not enabled, CLKEN2 can be used as a GP output controlled through I^2C accesses.

CLKREQ, when enabled, has a weak pulldown resistor to support the wired-OR clock request.

Figure 12-3 shows an example of the wired-OR clock request.

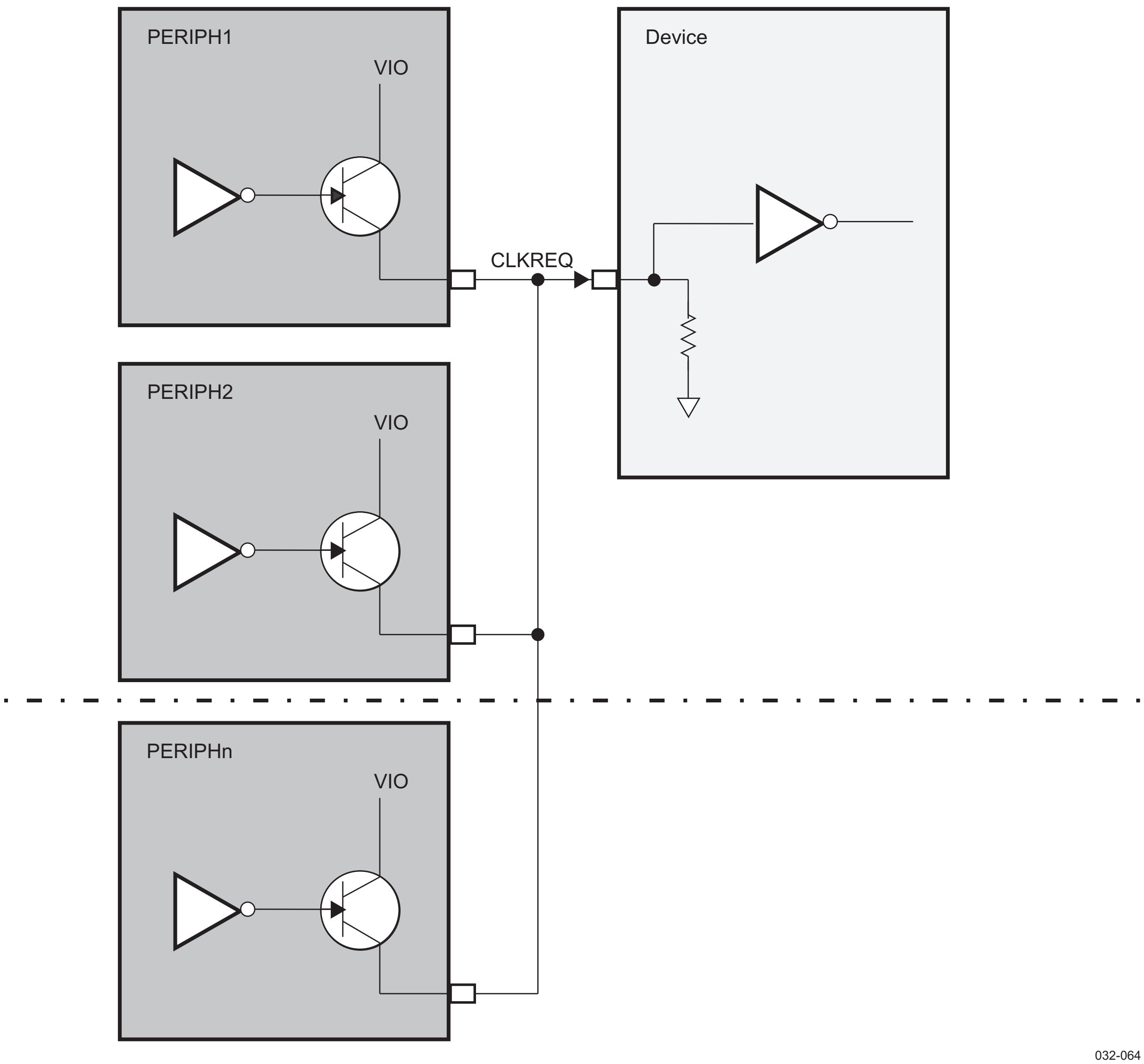


Figure 12-3. Example of Wired-OR Clock Request

NOTE

The timer default value must be the worst case (10 ms) for the clock providers. For legacy or workaround support, the signals NSLEEP1 and NSLEEP2 can also be used as a clock request even if it is not their primary goal. By default, this feature is disabled and must be enabled individually by setting the register bits associated with each signal.

When the external clock signal is present on the HFCLKIN ball, it is possible to use this clock instead of the internal RC oscillator and then synchronize the system on the same clock. The RC oscillator can then go to idle mode.

Table 12-2 lists the input clock electrical characteristics of the HFCLKIN input clock.

Table 12-2. HFCLKIN Input Clock Electrical Characteristics

Parameter	Configuration Mode Slicer	Min	Typ	Max	Unit
Frequency		19, 26, or 38.4			MHz
Startup time	LP/HP (sine wave)			4	µs
Input dynamic range	LP/HP (sine wave)	0.3	0.7	1.45	V_{PP}
	BP/PD (square wave)	0		1.8^{5} [1]	
Current consumption	LP			175	µA
	HP			235	
	BP/PD			39	nA
Harmonic content of input signal (with 0.7-V_{PP} amplitude): second component	LP/HP (sine wave)			–25	dBc
Voltage input high (V_{IH})	BP (square wave)	1			V
Voltage input low (V_{IL})	BP (square wave)			0.6	V

(1) Bypass input max voltage is the same as the maximum voltage provided for the I/O interface (IO.1P8V).

Table 12-3 lists the input clock timing requirements of the HFCLKIN input clock when the source is a square wave.

Table 12-3. HFCLKIN Square Input Clock Timing Requirements With Slicer in Bypass

Name	Parameter	Description	Min	Typ	Max	Unit
CH0	$1/t_{C(HFCLKIN)}$	Frequency, HFCLKIN	19.2, 26, or 38.4			MHz
CH1	$t_{W(HFCLKIN)}$	Pulse duration, HFCLKIN low or high	$0.45 * t_{C(HFCLKIN)}$		$0.55 * t_{C(HFCLKIN)}$	ns
CH3	$t_{R(HFCLKIN)}$	Rise time, HFCLKIN [1]			5	ns
CH4	$t_{F(HFCLKIN)}$	Fall time, HFCLKIN [1]			5	ns

(1) Default drive capability is 40 pF.

Figure 12-4 shows the timing of the HFCLKIN squared input clock.

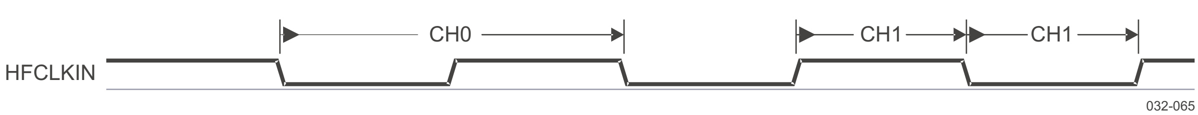


Figure 12-4. HFCLKIN Squared Input Clock

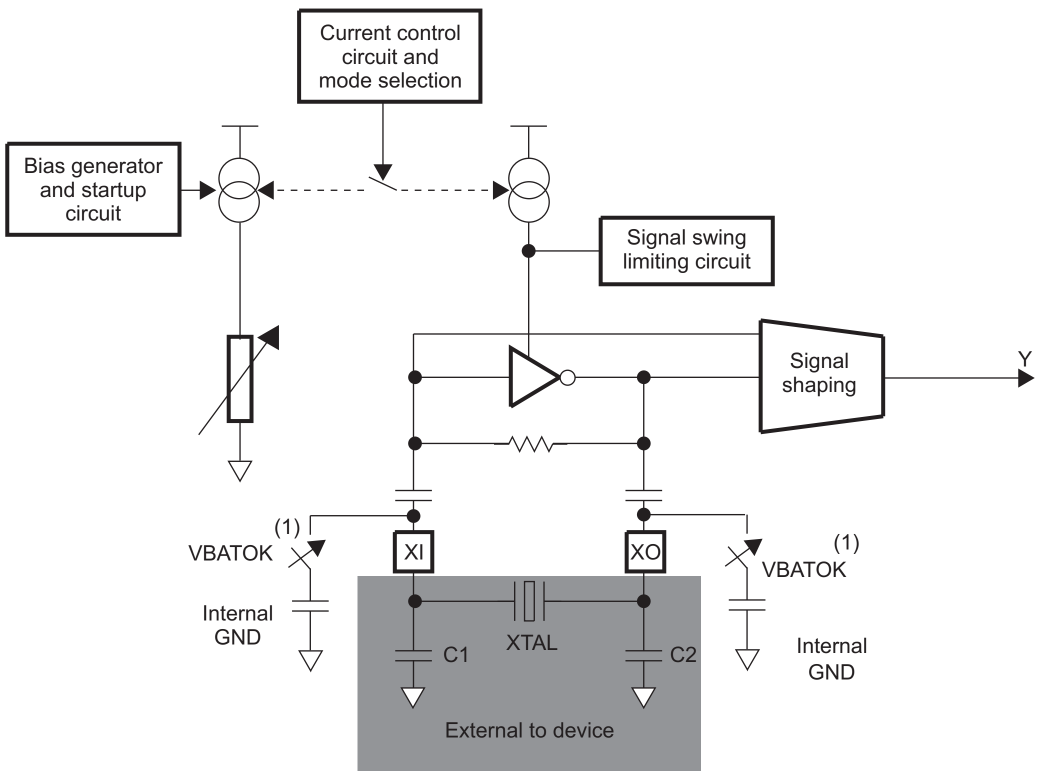
12.2.3 32-kHz Input Clock

A 32.768-kHz input clock (often abbreviated to 32-kHz) generates the clocks for the RTC. It has a low-jitter mode where the current consumption increases for lower jitter. It is possible to use the 32-kHz input clock with an external crystal or clock source. Depending on the mode, the 32K oscillator is configured as being either:

- An external 32.768-kHz crystal through the 32KXIN/32KXOUT balls (see Figure 12-5). This configuration is available for master mode only (for more information, see Section 13, *Timing Requirements and Switching Characteristics*).
- An external square or sine wave of 32.768 kHz through 32KXIN with amplitude of 1.8 or 1.85 V (see Figure 12-7, Figure 12-8, and Figure 12-9). This configuration is available for master and slave modes (for more information, see Section 13, *Timing Requirements and Switching Characteristics*).

12.2.3.1 External Crystal Description

Figure 12-5 is a block diagram of the 32-kHz oscillator with crystal in master mode.



NOTE: Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 12-5. 32-kHz Oscillator Block Diagram In Master Mode With Crystal

CXIN and CXOUT represent the total capacitance of the printed circuit board (PCB) and components, excluding the crystal. Their values depend on the datasheet of the crystal, the internal capacitors, and the parallel capacitor. The frequency of the oscillations depends on the value of the capacitors. The crystal must be in the fundamental mode of operation and parallel resonant.

NOTE

For the values of CXIN and CXOUT, see Table 15-1.

Table 12-4 lists the required electrical constraints.

Table 12-4. Crystal Electrical Characteristics

Parameter	Min	Typ	Max	Unit
Parallel resonance crystal frequency		32.768		kHz
Input voltage, Vin (normal mode)	1.0	1.3	1.55	V

Table 12-4. Crystal Electrical Characteristics (continued)

Parameter	Min	Typ	Max	Unit
Internal capacitor on each input (Cint)		10		pF
Parallel input capacitance (Cpin)			1	pF
Nominal load cap on each oscillator input CXIN and CXOUT (1)	CXIN = CXOUT = Cosc*2 – (Cint + Cpin)			pF
Pin-to-pin capacitance		1.6	1.8	pF
Crystal ESR (2)			75	kΩ
Crystal shunt capacitance, C_O			1	pF
Crystal tolerance at room temperature, 25°C	–30		30	ppm
Crystal tolerance versus temperature range (–40°C to 85°C)	–200		200	ppm
Maximum drive power			1	µW
Operating drive level			0.5	µW

(1) Nominal load capacitor on each oscillator input defined as CXIN = CXOUT = Cosc*2 – (Cint + Cpin). Cosc is the load capacitor defined in the crystal oscillator specification, Cint is the internal capacitor, and Cpin is the parallel input capacitor.
(2) The crystal motional resistance Rm relates to the equivalent series resistance (ESR) by the following formula:

$$ESR = R_m \left(1 + \frac{C_O}{C_L}\right)^2$$

Measured with the load capacitance specified by the crystal manufacturer. If CXIN = CXOUT = 10 pF, then C_L = 5 pF. Parasitic capacitance from the package and board must also be considered.

When selecting a crystal, the system design must consider the temperature and aging characteristics of a crystal versus the user environment and expected lifetime of the system.

Table 12-5 and Table 12-6 list the switching characteristics of the oscillator and the input requirements of the 32.768-kHz input clock, respectively. Figure 12-6 shows the crystal oscillator output in normal mode.

Table 12-5. Base Oscillator Switching Characteristics

Name	Parameter Description		Min	Typ	Max	Unit
f_P	Oscillation frequency			32.768		kHz
t_{SX}	Startup time				0.5	s
I_{DDA}	Active current consumption	LOJIT <1:0> = 00			1.8	µA
		LOJIT <1:0> = 11			8	
I_{DDQ}	Current consumption	Low battery mode (1.2 V)			1	µA
		Startup			8	

Table 12-6. 32-kHz Crystal Input Clock Timing Requirements

Name	Parameter Description		Min	Typ	Max	Unit
OC0	$1/t_{C(32KHZ)}$	Frequency, 32 kHz		32.768		kHz
OC1	$t_{W(32KHZ)}$	Pulse duration, 32 kHz low or high	$0.40*t_{C(32KHZ)}$		$0.60*t_{C(32KHZ)}$	µs

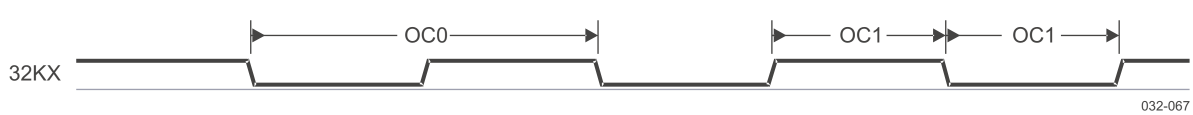
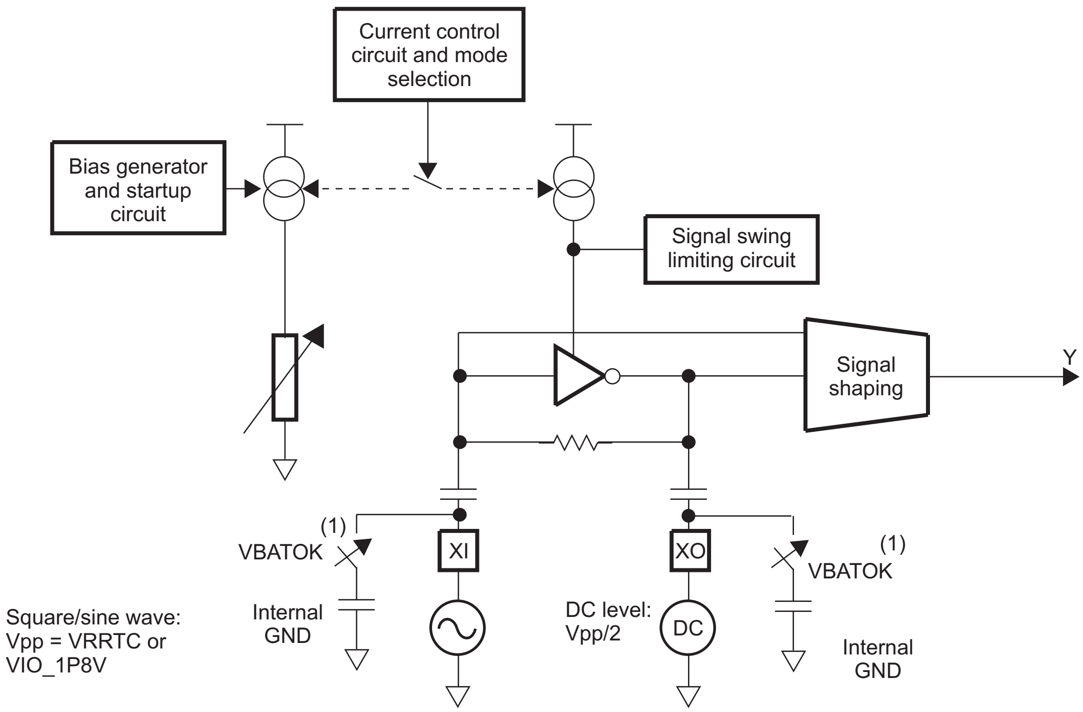


Figure 12-6. 32-kHz Crystal Input

12.2.3.2 External Clock Description

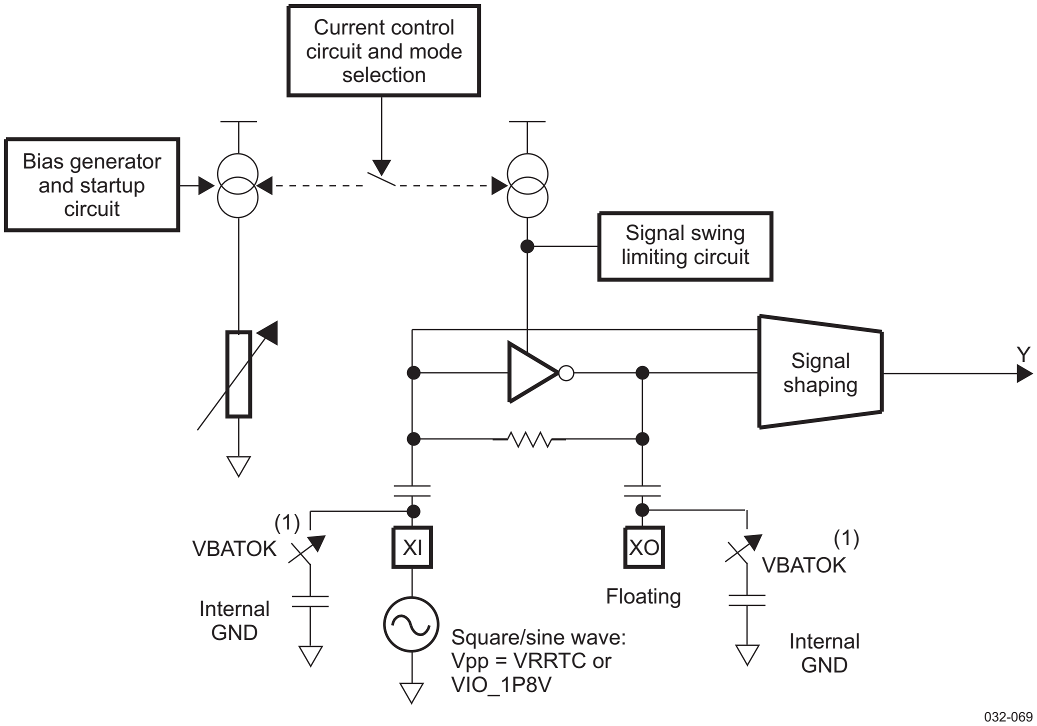
Figure 12-7 and Figure 12-8 show the 32-kHz oscillator with a 32.768-kHz square or sine signal in master and slave modes. Figure 12-9 shows an external clock source when the oscillator is configured in bypass mode. Thus, there are three configurations:

- A square- or sine-wave input can be applied to the 32KXIN pin with an amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be driven to a dc value of the square- or sine-wave amplitude divided by 2. This configuration, shown in Figure 12-7, is recommended if a large load is applied on the 32KXOUT pin.
- A square- or sine-wave input can be applied to the 32KXIN pin with an amplitude of 1.85 or 1.8 V. The 32KXOUT pin can be left floating. This configuration, showed in Figure 12-8, is used if no charge is applied on the 32KXOUT pin.
- The oscillator is in bypass mode and a square-wave input can be applied to the 32KXIN pin with an amplitude of 1.8 V. The 32KXOUT pin can be left floating. This configuration, shown in Figure 12-9, is used if the oscillator is in bypass mode.



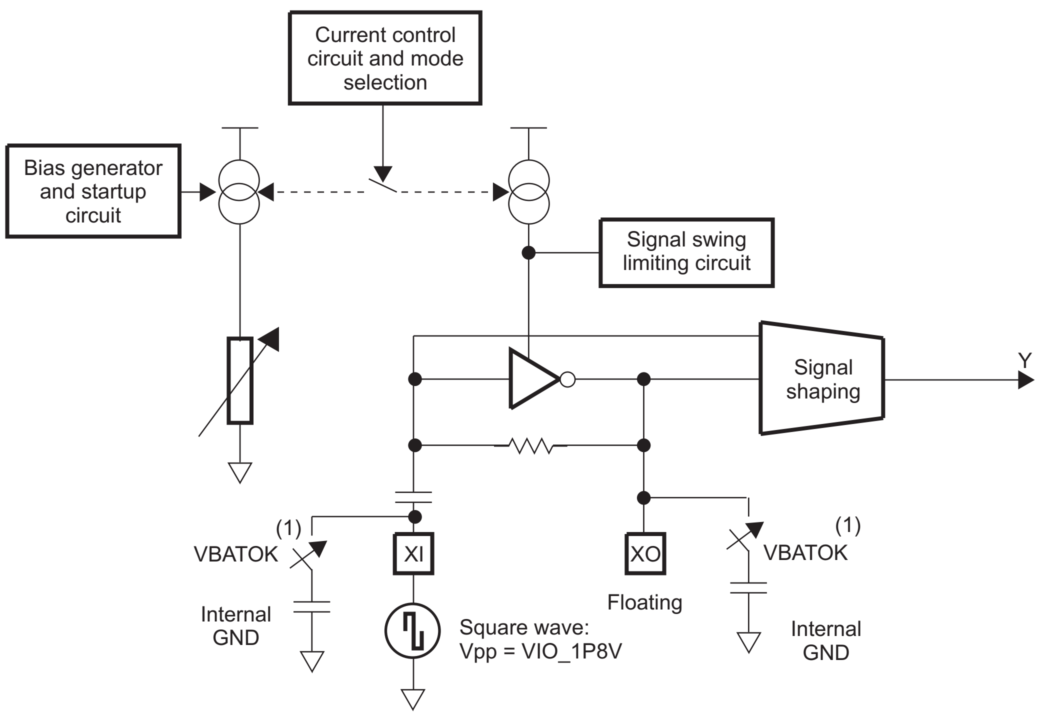
(1) Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 12-7. 32-kHz Oscillator Block Diagram Without Crystal Option 1



(1) Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 12-8. 32-kHz Oscillator Block Diagram Without Crystal Option 2



(1) Switches close by default and open only if register access enables very-low-power mode when VBAT < 2.7 V.

Figure 12-9. 32-kHz Oscillator in Bypass Mode Block Diagram Without Crystal Option 3

Table 12-7 lists the electrical constraints required by the 32-kHz input square- or sine-wave clock used.

Table 12-7. 32-kHz Input Square- or Sine-Wave Clock Source Electrical Characteristics

Name	Parameter Description	Min	Typ	Max	Unit
f	Frequency		32.768		kHz
C_I	Input capacitance		35		pF
C_{FI}	On-chip foot capacitance to GND on each input (see Figure 12-7, Figure 12-8, and Figure 12-9)		10		pF
V_{PP}	Square-/sine-wave amplitude in bypass mode or not		1.8 (1)		V
V_{IH}	Voltage input high, square wave in bypass mode	0.8			V
V_{IL}	Voltage input low, square wave in bypass mode			0.6	V

(1) Bypass input maximum voltage is the same as the maximum voltage provided for the I/O interface.

Table 12-8 lists the input requirements of the 32-kHz square-wave input clock.

Table 12-8. 32-kHz Square-Wave Input Clock Source Timing Requirements

Name	Parameter	Description	Min	Typ	Max	Unit
CK0	$1/t_{C(32KHZ)}$	Frequency, 32 kHz		32.768		MHz
CK1	$t_{W(32KHZ)}$	Pulse duration, 32 kHz low or high	$0.45*t_{C(32KHZ)}$		$0.55*t_{C(32KHZ)}$	μs
CK3	$t_{R(32KHZ)}$	Rise time, 32 kHz (1)			$0.1*t_{C(32KHZ)}$	μs
CK4	$t_{F(32KHZ)}$	Fall time, 32 kHz (1)			$0.1*t_{C(32KHZ)}$	μs

(1) The capacitive load is 30 pF.

Figure 12-10 shows the timing of the 32-kHz square- or sine-wave input clock.

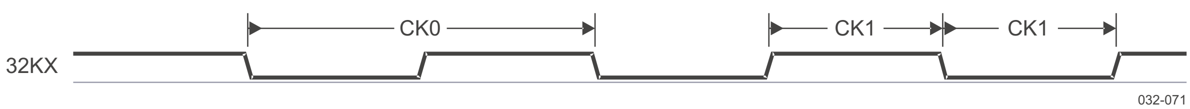


Figure 12-10. 32-kHz Square- or Sine-Wave Input Clock

12.3 Output Clock Specifications

The TPS65950 provides two output clocks:

- 32KCLKOUT
- HFCLKOUT

12.3.1 32KCLKOUT Output Clock

Figure 12-11 is a block diagram of the 32.768-kHz clock output.

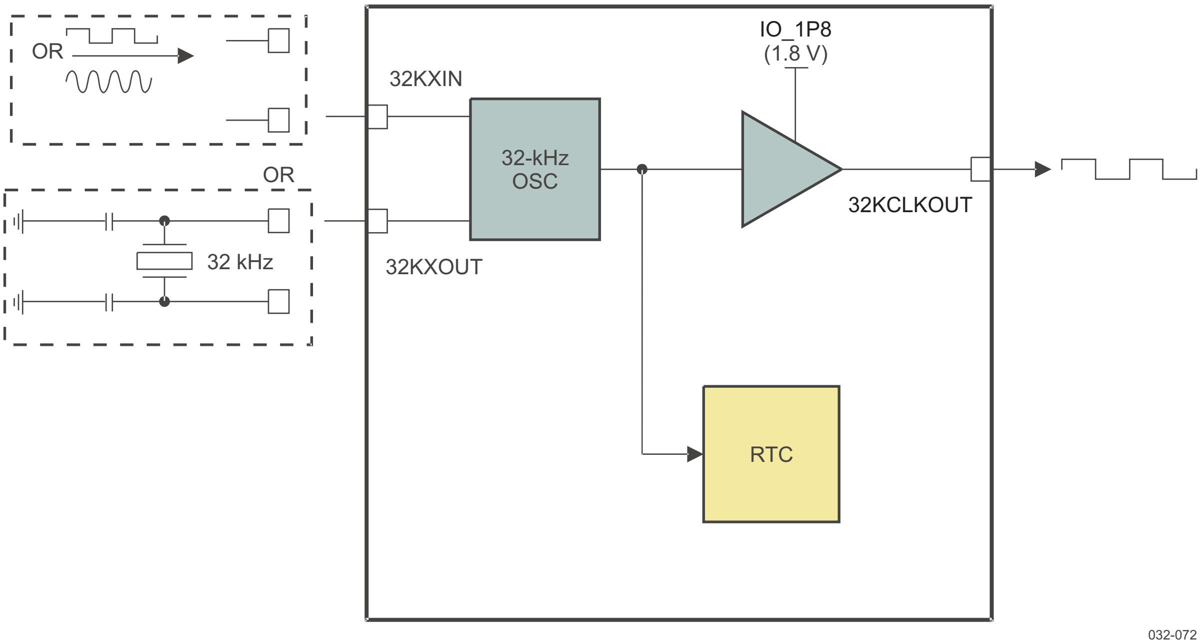


Figure 12-11. 32.768-kHz Clock Output Block Diagram

The TPS65950 has an internal 32.768-kHz oscillator connected to an external 32.768-kHz crystal through the 32KXIN/32KXOUT balls or an external digital 32.768-kHz clock through the 32KXIN input (see Figure 12-11). The TPS65950 also generates a 32.768-kHz digital clock through the 32KCLKOUT pin and can broadcast it externally to the application processor or any other devices. The 32KCLKOUT clock is broadcast by default in the TPS65950 active mode, but can be disabled if it is not used.

The 32.768-kHz clock (or signal) also clocks the RTC embedded in the TPS65950. The RTC is not enabled by default. The host processor must set the correct date and time and enable the RTC.

The 32KCLKOUT output buffer can drive several devices (up to a 40-pF load). At startup, the 32.768-kHz output clock (32KCLKOUT) must be stabilized (frequency/duty cycle) before the signal output. Depending on the startup condition, this can delay the startup sequence.

Table 12-9 lists the electrical characteristics of the 32KCLKOUT output clock.

Table 12-9. 32KCLKOUT Output Clock Electrical Characteristics

Name	Parameter Description	Min	Typ	Max	Unit
f	Frequency		32.768		kHz
C_L	Load capacitance			40	pF
V_{OUT}	Output clock voltage, depending on output reference level IO_1P8 (see Section 2)		1.8(1)		V
V_{OH}	Voltage output high	V_{OUT} – 0.45		V_{OUT}	V
V_{OL}	Voltage output low	0		0.45	V

(1) The output voltage depends on output reference level, which is IO_1P8 (see Section 2, *Terminal Description*).

Table 12-10 lists the timing characteristics of the 32KCLKOUT output clock. Figure 12-12 shows the waveform of the 32KCLKOUT output clock.

Table 12-10. 32KCLKOUT Output Clock Switching Characteristics

Name	Parameter	Description	Min	Typ	Max	Unit
CK0	$1/t_{C(32KCLKOUT)}$	Frequency		32.768		MHz
CK1	$t_{W(32KCLKOUT)}$	Pulse duration, 32KCLKOUT low or high	$0.40*t_{C(32KCLKOUT)}$		$0.60*t_{C(32KCLKOUT)}$	ns

Table 12-10. 32KCLKOUT Output Clock Switching Characteristics (continued)

Name	Parameter	Description	Min	Typ	Max	Unit
CK2	$t_{R(32KCLKOUT)}$	Rise time, 32KCLKOUT[1]			16	ns
CK3	$t_{F(32KCLKOUT)}$	Fall time, 32KCLKOUT[1]			16	ns

(1) The output capacitive load is 30 pF.

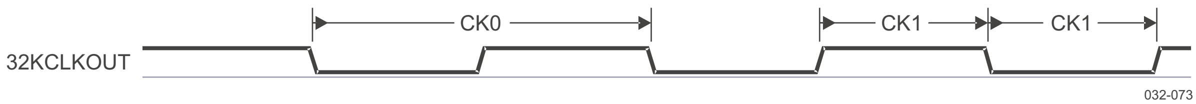


Figure 12-12. 32KCLKOUT Output Clock

12.3.2 HFCLKOUT Output Clock

Table 12-11 lists the electrical characteristics of the HFCLKOUT output clock.

Table 12-11. HFCLKOUT Output Clock Electrical Characteristics

Name	Parameter Description	Min	Typ	Max	Unit
f	Frequency		19.2, 26, or 38.4		MHz
C_L	Load capacitance			30	pF
V_{OUT}	Output clock voltage, depending on output reference level IO_1P8 (see Section 2)		1.8[1]		V
V_{OH}	Voltage output high	V_{OUT} – 0.45		V_{OUT}	V
V_{OL}	Voltage output low	0		0.45	V

(1) The output voltage depends on output reference level, which is IO_1P8 (see Section 2).

Table 12-12 lists the timing characteristics of the HFCLKOUT output clock.

Table 12-12. HFCLKOUT Output Clock Switching Characteristics

Name	Parameter	Description	Min	Typ	Max	Unit
CHO1	$1/t_{C(HFCLKOUT)}$	Frequency		19.2, 26, or 38.4		MHz
CHO2	$t_{W(HFCLKOUT)}$	Pulse duration, HFCLKOUT low or high	$0.40*t_{C(HFCLKOUT)}$		$0.60*t_{C(HFCLKOUT)}$	ns
CHO3	$t_{R(HFCLKOUT)}$	Rise time, HFCLKOUT[1]			2.6	ns
CHO4	$t_{F(HFCLKOUT)}$	Fall time, HFCLKOUT[1]			2.6	ns

(1) The output capacitive load is 30 pF.

Figure 12-13 shows the waveform of the HFCLKOUT output clock.

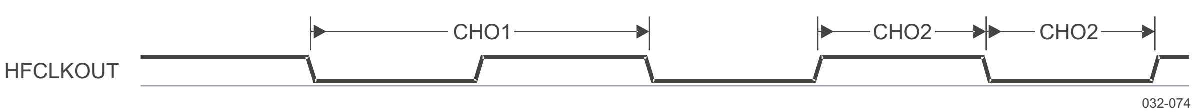
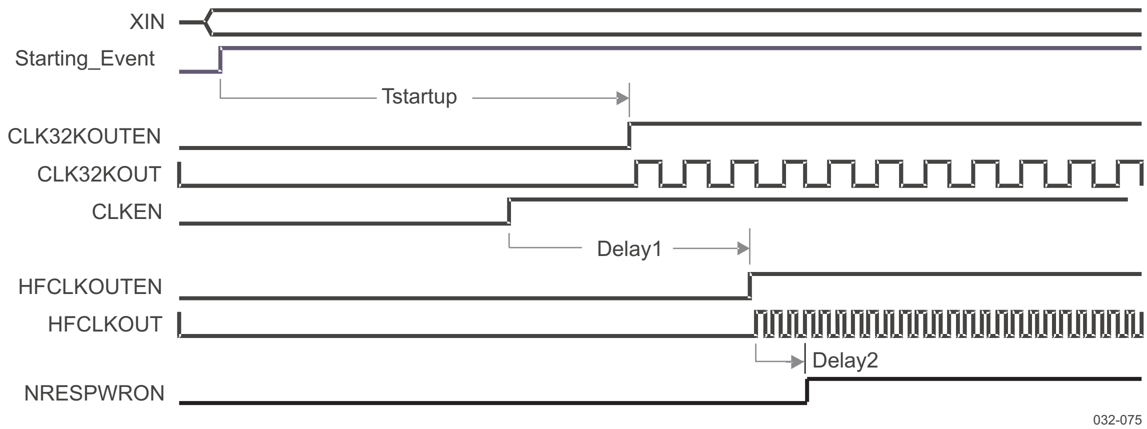


Figure 12-13. HFCLKOUT Output Clock

12.3.3 Output Clock Stabilization Time

Figure 12-14 shows the 32KCLKOUT and HFCLKOUT clock stabilization time.



NOTE: Tstartup, Delay1, and Delay2 depend on the boot mode (see Section 4.5, *Power Management*).

NOTE: Ensure that the high frequency oscillator start-up time is in spec for the boot mode used. During power-up the internal delay, Delay1 above is fixed (5.2 ms and 5.3 ms depending on boot mode). The start-up time for the oscillator must be less than the fixed delay.

Figure 12-14. 32KCLKOUT and HFCLKOUT Clock Stabilization Time

Figure 12-15 shows the behavior of HFLCKOUT.

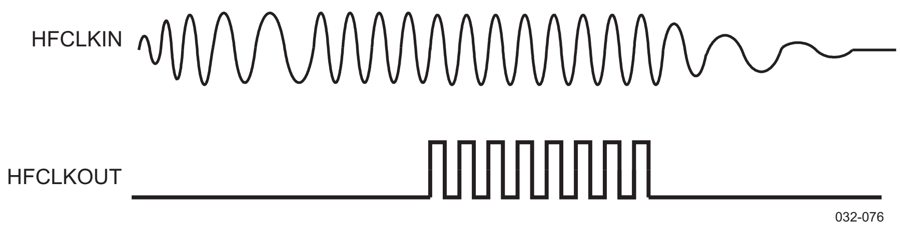


Figure 12-15. HFCLKOUT Behavior

13 Timing Requirements and Switching Characteristics

13.1 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies are abbreviated as shown in Table 13-1.

Table 13-1. Timing Parameters

Lowercase Subscripts	
Symbol	**Parameter**
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start-bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
H	High
L	Low
V	Valid
IV	Invalid
AE	Active edge
FE	First edge
LE	Last edge
Z	High impedance

13.2 Target Frequencies

Table 13-2 assumes testing over the recommended operating conditions.

Table 13-2. TPS65950 Interface Target Frequencies

I/O Interface	Interface Designation		Target Frequency
			1.5 V
SmartReflex I^2C GP I^2C	I^2C interface	Slave HS mode	3.6 Mbps
		Slave fast-speed mode	400 kbps
		Slave standard mode	100 kbps
USB	USB	HS	480 Mbps
		FS	12 Mbps
		LS	1.5 Mbps
JTAG	RealView® ICE tool		30 MHz
	XDS560 and XDS510 tools		30 MHz
	Lauterbach™ tool		30 MHz

Table 13-2. TPS65950 Interface Target Frequencies (continued)

I/O Interface	Interface Designation	Target Frequency 1.5 V
TDM/I2S	Inter-IC sound (I2S™)	1/(64 * Fs)(1)
	Right-justified	1/(64 * Fs)(1)
	Left-justified	1/(64 * Fs)(1)
	TDM	1/(128 * Fs)(1)
Voice/Bluetooth PCM interface	PCM (master mode)	1/(65 * Fs)(2)
	PCM (slave mode)	1/(33 to 65 * Fs)(2)

(1) Fs = 8 to 48 kHz; 96 kHz for RX path only (TDM/I2S interface)
(2) Fs = 8 or 16 kHz (voice/Bluetooth PCM interface)

13.3 I^{2}C Timing

The TPS65950 provides two I^{2}C HS slave interfaces (one for GP and one for SmartReflex). These interfaces support the standard mode (100 kbps), fast mode (400 kbps), and HS mode (3.4 Mbps). The GP I^{2}C module embeds four slave hard-coded addresses (ID1 = 48h, ID2 = 49h, ID3 = 4Ah, and ID4 = 4Bh). The SmartReflex I^{2}C module uses one slave hard-coded address (ID5). Master mode is not supported.

Table 13-3 and Table 13-4 assume testing over the recommended operating conditions (see Figure 13-1).

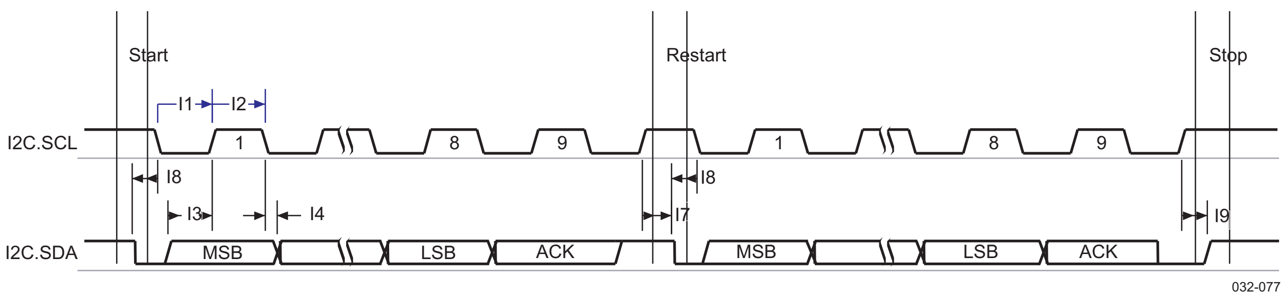


Figure 13-1. I^{2}C Interface—Transmit and Receive in Slave Mode

Table 13-3. I^{2}C Interface Timing Requirements(1) (2)

Notation	Parameter		Min	Max	Unit
Slave HS Mode					
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	10		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	70	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	160		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	160		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	160		ns
Slave Fast-Speed Mode					
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	100		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0	0.9	ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	0.6		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	0.6		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	0.6		ns

(1) The input timing requirements are given by considering a rising or falling time of:
80 ns in HS mode (3.4 Mbps)
300 ns in fast-speed mode (400 Kbps)
1000 ns in standard mode (100 Kbps)
(2) SDA equals I2C.SR.SDA or I2C.CNTL.SDA
SCL equals I2C.SR.SCL or I2C.CNTL.SCL

Table 13-3. I²C Interface Timing Requirements (continued)

Notation	Parameter		Min	Max	Unit
Slave Standard Mode					
I3	$t_{su(SDA-SCLH)}$	Setup time, SDA valid to SCL high	250		ns
I4	$t_{h(SCLL-SDA)}$	Hold time, SDA valid from SCL low	0		ns
I7	$t_{su(SCLH-SDAL)}$	Setup time, SCL high to SDA low	4.7		ns
I8	$t_{h(SDAL-SCLL)}$	Hold time, SCL low from SDA low	4		ns
I9	$t_{su(SDAH-SCLH)}$	Setup time, SDA high to SCL high	4		ns

Table 13-4. I²C Interface Switching Requirements(1) (2)

Notation	Parameter		Min	Max	Unit
Slave HS Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	160		ns
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	60		ns
Slave Fast-Speed Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	1.3 (3)		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	0.6		µs
Slave Standard Mode					
I1	$t_{w(SCLL)}$	Pulse duration, SCL low	4.7		µs
I2	$t_{w(SCLH)}$	Pulse duration, SCL high	4		µs

(1) The capacitive load is:
100 pF in HS mode (3.4 Mbps)
400 pF in fast-speed mode (400 Kbps)
400 pF in standard mode (100 Kbps)
(2) SDA equals I2C.SR.SDA or I2C.CNTL.SDA
SCL equals I2C.SR.SCL or I2C.CNTL.SCL
(3) SCL low timing for slave fast-speed mode is compatibile with 0.79 µs.

13.4 Audio Interface: TDM/I2S Protocol

The TPS65950 acts as a master for the TDM and I2S interface or as a slave only for the I2S interface. If the TPS65950 is the master, it must provide frame synchronization (TDM/I2S_SYNC) and bit clock (TDM/I2S_CLK) to the host processor. If the TPS65950 is the slave, it receives frame synchronization and bit clock.

The TPS65950 supports the I2S, TDM, left-justified, and right-justified data formats, but does not support TDM slave mode.

13.4.1 I2S Right- and Left-Justified Data Format

Table 13-5 and Table 13-6 assume testing over the recommended operating conditions (see Figure 13-2 and Figure 13-3).

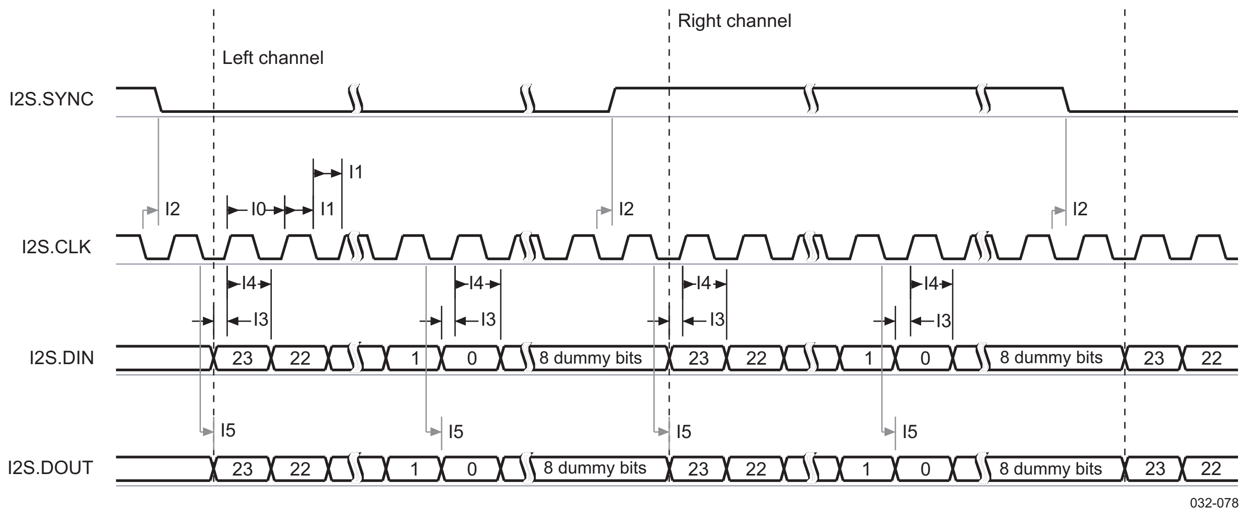


Figure 13-2. I2S Interface—I2S Master Mode

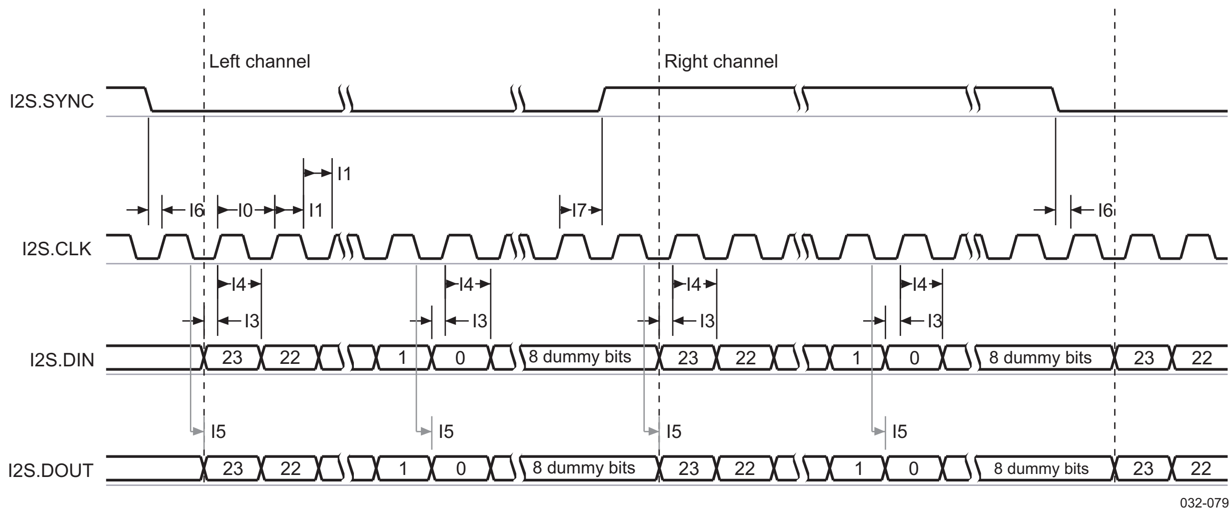


Figure 13-3. I2S Interface—I2S Slave Mode

The timing requirements in Table 13-5 are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is t_R/t_F = 1.0 ns/6.5 ns
- Capacitance load range of outputs (CLK, SYNC, DOUT) is C_{Load} = 1 pF/30 pF

The input timing requirements in Table 13-5 are given by considering a rising or falling time of 6.5 ns.

Table 13-5. I2S Interface—Timing Requirements

Notation	Parameter		Min	Max	Unit
Master Mode					
I3	$t_{su(DIN-CLKH)}$	Setup time, I2S.DIN valid to I2S.CLK high2	25		ns
I4	$t_{h(DIN-CLKH)}$	Hold time, I2S.DIN valid from I2S.CLK high.	0		ns
Slave Mode					
I0	$t_{c(CLK)}$	Cycle time, I2S.CLK(1)	1/64 * Fs		ns
I1	$t_{w(CLK)}$	Pulse duration, I2S.CLK high or low(2)	0.45 * P	0.55 * P	ns

(1) Fs = 8 to 48 kHz; 96 kHz for RX path only
(2) P = I2S.CLK period

Table 13-5. I2S Interface—Timing Requirements (continued)

Notation	Parameter		Min	Max	Unit
I3	$t_{su(DIN-CLKH)}$	Setup time, I2S.DIN valid to I2S.CLK high	5		ns
I4	$t_{h(DIN-CLKH)}$	Hold time, I2S.DIN valid from I2S.CLK high.	5		ns
I6	$t_{su(SYNC-CLKH)}$	Setup time, I2S.SYNC valid to I2S.CLK high	5		ns
I7	$t_{h(SYNC-CLKH)}$	Hold time, I2S.SYNC valid from I2S.CLK high	5		ns

The capacitive load for Table 13-6 is 7 pF.

Table 13-6. I2S Interface—Switching Characteristics

Notation	Parameter		Min	Max	Unit
Master Mode					
I0	$t_{c(CLK)}$	Cycle time, I2S.CLK(1)	1/64 * Fs		ns
I1	$t_{w(CLK)}$	Pulse duration, I2S.CLK high or low(2)	0.45 * P	0.55 * P	ns
I2	$t_{d(CLKL-SYNC)}$	Delay time, I2S.CLK falling edge to I2S.SYNC transition	–10	10	ns
I5	$t_{d(CLKL-DOUT)}$	Delay time, I2S.CLK falling edge to I2S.DOUT transition	–10	10	ns
Slave Mode					
I5	$t_{d(CLKL-DOUT)}$	Delay time, I2S.CLK falling edge to I2S.DOUT transition	0	20	ns

(1) Fs = 8 to 48 kHz; 96 kHz for RX path only
(2) P = I2S.CLK period

13.4.2 TDM Data Format

Table 13-7 and Table 13-8 assume testing over the recommended operating conditions (see Figure 13-4).

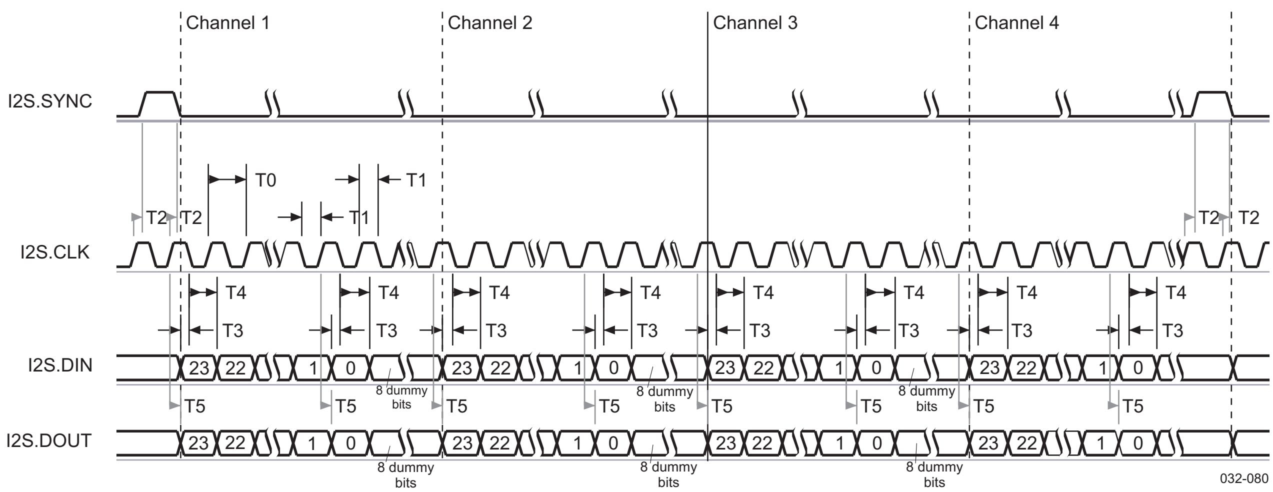


Figure 13-4. TDM Interface—TDM Master Mode

The timing requirements in Table 13-7 are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is t_R/t_F = 1.0 ns/6.5 ns
- Capacitance load range of outputs (CLK, SYNC, DOUT) is C_{Load} = 1 pF/30 pF

Table 13-7 lists the master mode timing requirements for the TDM interface.

Table 13-7. TDM Interface Master Mode Timing Requirements

Notation	Parameter		Min	Max	Unit
T3	$t_{su(DIN-CLKH)}$	Setup time, TDM.DIN valid to TDM.CLK high	25		ns
T4	$t_{h(DIN-CLKH)}$	Hold time, TDM.DIN valid from TDM.CLK high	0		ns

Table 13-8 lists the master mode switching characteristics of the TDM interface.

Table 13-8. TDM Interface Master Mode Switching Characteristics

Notation	Parameter		Min	Max	Unit
T0	$t_{c(CLK)}$	Cycle time, TDM.CLK (1)	1/64 * Fs		ns
T1	$t_{w(CLK)}$	Pulse duration, TDM.CLK high or low(2)	0.45*P	0.55*P	ns
T2	$t_{d(CLKL-SYNC)}$	Delay time, TDM.CLK rising edge to TDM.SYNC transition	–10	10	ns
T5	$t_{d(CLKL-DOUT)}$	Delay time, TDM.CLK rising edge to TDM.DOUT transition	–10	12	ns

(1) Fs = 8 to 48 kHz; 96 kHz for RX path only
(2) P = TDM.CLK period

13.5 Voice/Bluetooth PCM Interfaces

The PCM interface transfers voice data at 8-kHz (default narrowband mode) or 16-kHz (wideband mode) sample rates. The CM interface can act as a slave or master. No PLL is used for the PCM interface, but dividers are used to derive the 8- or 16-kHz clock from HFCLKIN (only when HFCLKIN = 26 MHz). If the system master clock is not 26 MHz, the voice PCM interface is not available.

For the Bluetooth interface, the PCM is supported to transfer voice data to the Bluetooth chip at 8-kHz (default narrowband mode) or 16-kHz sample rate.

The TPS65950 acts as a master for the Bluetooth interface. The frame synchronization and the bit clock are shared from the voice PCM interface. If the system master clock is not 26 MHz, the Bluetooth interface is not available.

Two modes are available for the PCM interfaces: mode 1 (writing on the PCM_VCK rising edge) and mode 2 (writing on the PCM_VCK falling edge).

Table 13-9 and Table 13-10 assume testing over the recommended operating conditions (see Figure 13-5 and Figure 13-6).

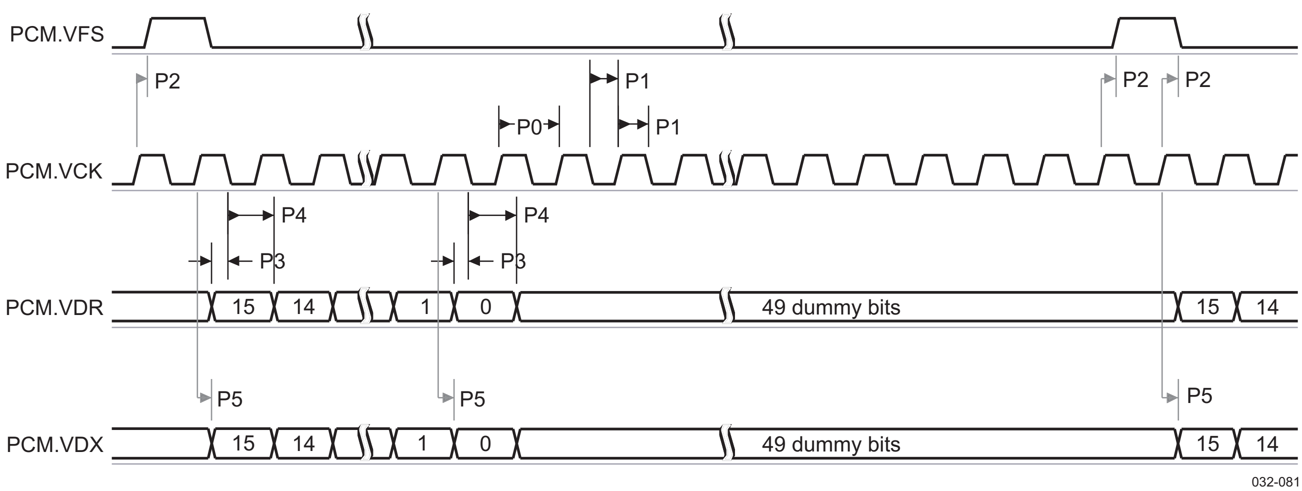


Figure 13-5. Voice/BT PCM Interface—Master Mode (Mode 1)

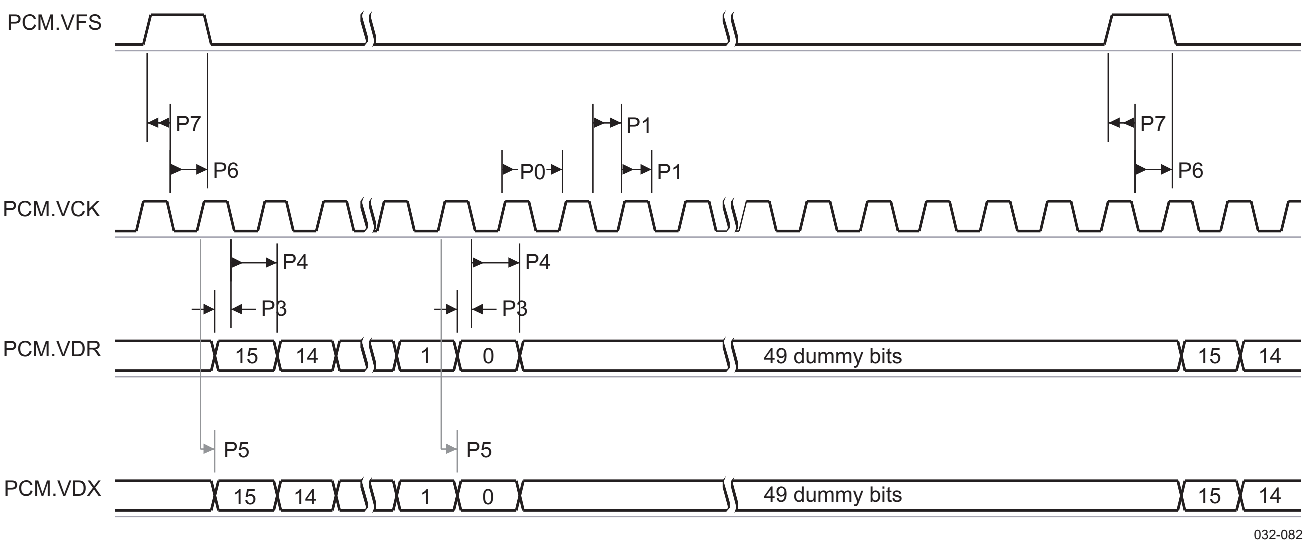


Figure 13-6. Voice PCM Interface—Slave Mode (Mode 1)

The timing requirements in Table 13-9 are valid on the following conditions of input slew and output load:

- Rise and fall time range of inputs (SYNC, DIN) is t_R/t_F = 1.0 ns/6.5 ns
- Capacitance load range of outputs (CLK, SYNC, DOUT) is C_{Load} = 1 pF/30 pF

Table 13-9 lists the timing requirements for the voice PCM interface, mode 1.

Table 13-9. Voice PCM Interface Timing Requirements (Mode 1)

Notation	Parameter		Min	Max	Unit
Voice/Bluetooth PCM Master Mode					
P3	$t_{su(VDR-VCK)}$	Setup time, PCM.VDR valid to PCM. VCK transition (1)	30		ns
P4	$t_{h(VDR-VCK)}$	Hold time, PCM.VDR valid from PCM.VCK transition (1)	0		ns
Voice PCM Slave Mode					
P0	$t_{c(VCK)}$	Cycle time, PCM.VCK (2)	1/(33 to 65 * Fs)		ns
P1	$t_{w(VCK)}$	Pulse duration, PCM.VCK high or low (3)	0.45 * P	0.55 * P	ns
P3	$t_{su(VDR-VCK)}$	Setup time, PCM.VDR valid to PCM. VCK transition (1)	10		ns
P4	$t_{h(VDR-VCK)}$	Hold time, PCM.VDR valid from PCM. VCK transition (1)	5		ns
P6	$t_{h(VFS-VCK)}$	Hold time, PCM.VFS valid from PCM.VCK transition (1)	5		ns
P7	$t_{SU(VFS-VCK)}$	Setup time, PCM.VFS valid to PCM. VCK transition (1)	10		ns

(1) Writing on PCM.VCK rising edge (mode 1) and writing on PCM.VCK falling edge (mode 2).
(2) Fs = 8 or 16 kHz
(3) P = PCM.CLK period

Table 13-10 lists the switching characteristics of the voice PCM interface, mode 1.

Table 13-10. Voice PCM Interface Switching Characteristics (Mode 1)

Notation	Parameter		Min	Max	Unit
Voice/Bluetooth PCM Master Mode					
P0	$t_{c(VCK)}$	Cycle time, PCM.VCK (1)	1/65 * Fs		ns
P1	$t_{w(VCK)}$	Pulse duration, PCM.VCK high or low (2)	0.45 * P	0.55 * P	ns

(1) Fs = 8 or 16 kHz
(2) P = PCM.CLK period

Table 13-10. Voice PCM Interface Switching Characteristics (Mode 1) (continued)

Notation	Parameter		Min	Max	Unit
P2	$t_{d(VCK-VFS)}$	Delay time, PCM.VCK transition to PCM.VFS transition (3)	–10	10 + Pvoice	ns
P5	$t_{d(VCL-VDX)}$	Delay time, PCM.VCK transition to PCM.VDX transition	–10	10	ns
Voice PCM Slave Mode					
P5	$t_{d(VCL-VDX)}$	Delay time, PCM.VCK transition to PCM.VDX transition	0	20	ns

(3) When TPS65950 is master, the PCM.VFS is delivered one cycle time of 26-MHz voice clock (Pvoice=38.4 ns) after the PCM.VCK rising edge.

13.6 JTAG Interfaces

The TPS65950 Joint Test Action Group (JTAG) test access port (TAP) controller handles standard IEEE JTAG interfaces. This section describes the timing requirements for the tools used to test TPS65950 power management.

The JTAG/TAP module provides a JTAG interface according to IEEE Standard 1149.1a. This interface uses the four I/O pins TMS, TCK, TDI, and TDO. The TMS, TCK, and TDI inputs contain a pullup device, which makes their state high when they are not driven. The output TDO is a 3-state output, which is high impedance except when data are shifted between TDI and TDO:

- TCK is the test clock signal.
- TMS is the test mode select signal.
- TDI is the scan path input.
- TDO is the scan path output.

TMS and TDO are multiplexed at the top level with the GPIO0 and GPIO1 pins. The dedicated external test pin switches from functional mode (GPIO0 and GPIO1) to JTAG mode (TMS and TDO). The JTAG operations are controlled by a state-machine that follows the IEEE Standard 1149.1a state diagram. This state-machine is reset by the TPS65950 internal power-on reset (POR). A test mode is selected by writing a 6-bit word (instruction) into the instruction register and then accessing the related data register.

Table 13-11 and Table 13-12 assume testing over the recommended operating conditions (see Figure 13-7). The input timing requirements are given by considering a rising or falling edge of 7 ns. The capacitive load is 35 pF.

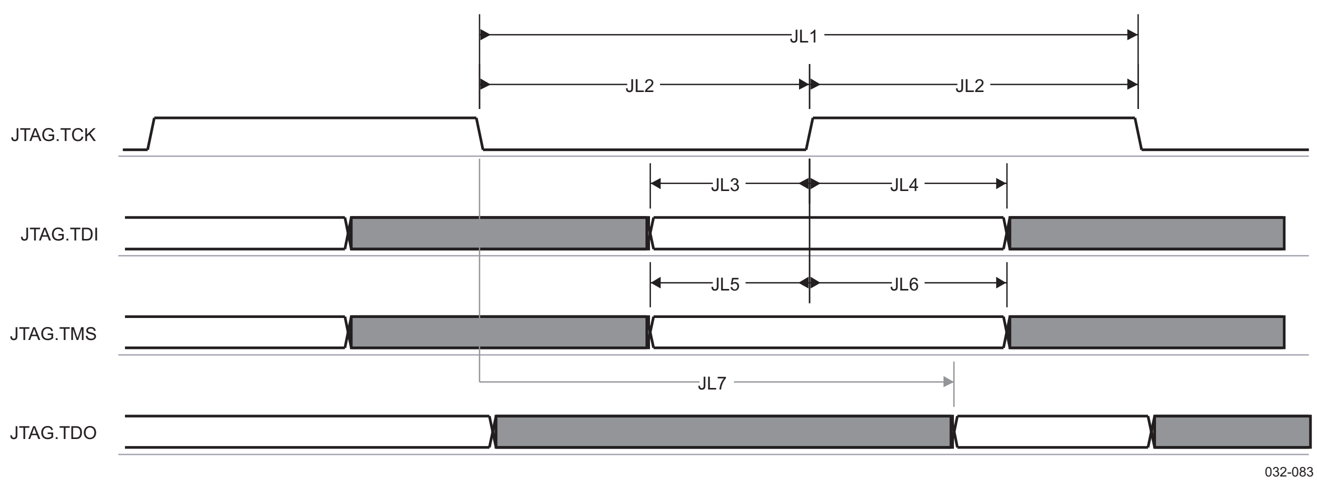


Figure 13-7. JTAG Interface Timing

Table 13-11. JTAG Interface Timing Requirements

Notation	Parameter		Min	Max	Unit
Clock					
JL1	$t_{c(TCK)}$	Cycle time, JTAG.TCK period	30		ns
JL2	$t_{w(TCK)}$	Pulse duration, JTAG.TCK high or low(1)	0.48*P	0.52*P	ns
Read Timing					
JL3	$t_{su(TDIV-TCKH)}$	Setup time, JTAG.TDI valid before JTAG.TCK high	8		ns
JL4	$t_{h(TDIV-TCKH)}$	Hold time, JTAG.TDI valid after JTAG.TCK high	5		ns
JL5	$t_{su(TMSV-TCKH)}$	Setup time, JTAG.TMS valid before JTAG.TCK high	8		ns
JL6	$t_{h(TMSV-TCKH)}$	Hold time, JTAG.TMS valid after JTAG.TCK high	5		ns

(1) P = JTAG.TCK clock period

Table 13-12. JTAG Interface Switching Characteristics

Notation	Parameter		Min	Max	Unit
Write Timing					
JL7	$t_{d(TCK-TDOV))}$	Delay time, JTAG, TCK active edge to JTAG.TDO valid	0	14	ns

14 Debouncing Time

Table 14-1 lists the debouncing functions.

Table 14-1. Debouncing Time

Debouncing Functions	Block	Programmable	Debouncing Time	Default
Main battery charged threshold (<3.2 V)	Battery monitoring	No	580 µs	580 µs
Main battery low threshold detection (<2.7 V)		No	60 µs	60 µs
Main battery plug detection (with charger connected)		No	60 µs	60 µs
Charger unplug detection (1)	BCI (automatic charge)	No	1 x 50 ms	1 x 50 ms
Charger plug detection (1)	BCI	No	9 x 50 ms	9 x 50 ms
Debouncing functions interrupt generation debounce for charger plug	Power	No	125.6 µs	125.6 µs
USB plug detection/VBUS precharge (same debouncing as charger plug) (1)	BCI	No	9 x 50 ms	9 x 50 ms
Battery presence plug/unplug (1)	BCI	No	9 x 50 ms	9 x 50 ms
Battery thermistor in/out of range (1)	BCI	No	4 x 50 ms	4 x 50 ms
Plug/unplug detection VBUS (2)	USB	Yes	0 to 250 ms (32/32,468-second steps)	28 ms
Plug/unplug detection ID (3)	USB	Yes	0 to 250 ms (32/32,468-second steps)	50 ms
Debouncing functions interrupt generation debounce for VBUS and ID (4)	Power	Yes	0 to 250 ms	30 ms
Hot-die detection	Thermistor	No	60 µs	60 µs
Thermal shutdown detection		No	60 µs	60 µs
PWRON (5)	Start/stop button	No	31.25 ms	31.25 ms
NRESWARM	Button reset	No	60 µs	60 µs
SIM card plug/unplug	GPIO	Yes	0 or 30 ms ± 1 ms	0 ms
Headset detection (plug/unplug)	GPIO	Yes	0 or 30 ms ± 1 ms	0 ms
MMC1/2 (plug/unplug)	GPIO	Yes	0 or 30 ms ± 1 ms	0 ms

(1) According to the capture of the event, debouncing time can vary between 50 ms and 50 ms + dT (dT included in 0 < dT > 50 ms). Figure 14-1 shows and explains this possible variation of the debouncing time.
(2) Programmable in the VBUS_DEBOUNCE register
(3) Programmable in the ID_DEBOUNCE register
(4) Programmable in the RESERVED_E[2:0] CFG_VBUSDEB register
(5) The PWRON signal is debounced 1024 × CLK32K (maximum 1026 × CLK32K) falling edge in master mode.

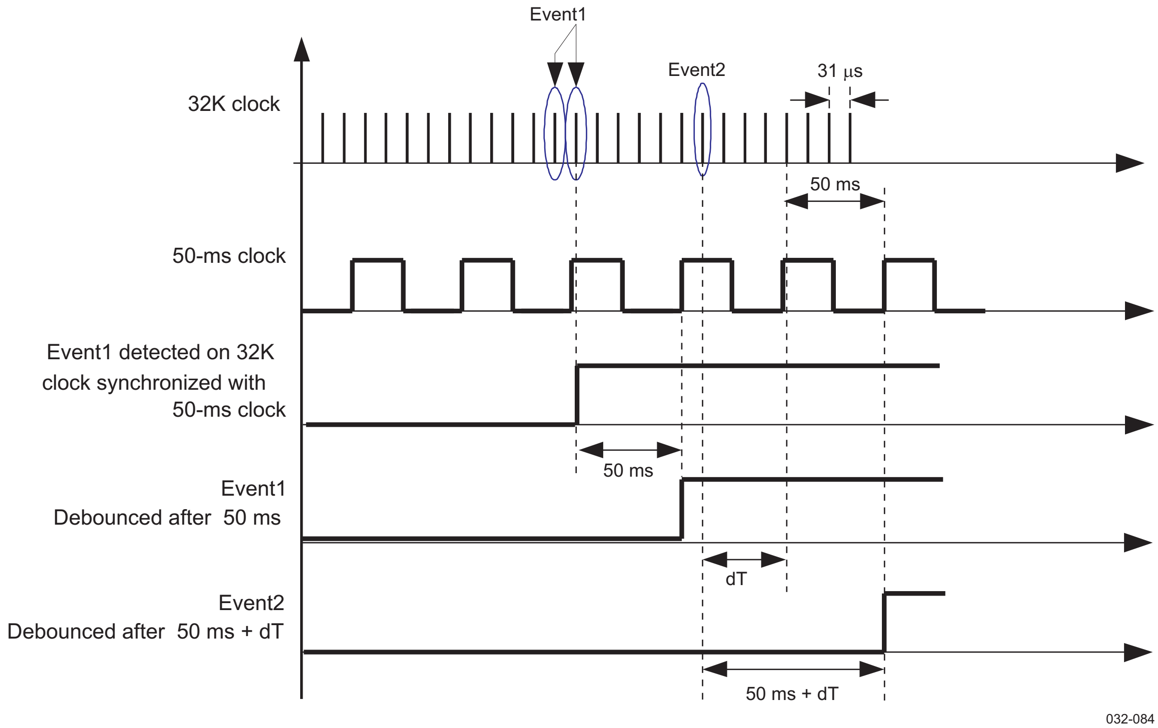


Figure 14-1. Debouncing Sequence Chronogram Example

Event 1 is correctly debounced after 50 ms. Event 2 is debounced after 50 ms + dT because the capture of the event is considered after the next rising edge of the 50-ms clock.

15 External Components

Table 15-1 lists the external components of the TPS65950.

Table 15-1. TPS65950 External Components

Function	Component	Reference	Value	Note	Link
Power Supplies					
VDD1	Capacitor	$C_{VDD1.IN}$	10 μF	Range ± 50% ESR minimum = 1 mΩ ESR maximum = 20 mΩ Taiyo Yuden: JMK212BJ106KD	Figure 4-1
	Capacitor	$C_{VDD1.OUT}$	10 μF	Range ± 50% ESR minimum = 1 mΩ ESR maximum = 20 mΩ Taiyo Yuden: JMK212BJ106KD	
	Inductor	L_{VDD1}	1 μH	Range ± 30% DCR maximum = 100 mΩ	
VDD2	Capacitor	$C_{VDD2.IN}$	10 μF	Range ± 50% ESR minimum = 1 mΩ ESR maximum = 20 mΩ Taiyo Yuden: JMK212BJ106KD	Figure 4-1
	Capacitor	$C_{VDD2.OUT}$	10 μF	Range ± 50% ESR minimum = 1 mΩ ESR maximum = 20 mΩ Taiyo Yuden: JMK212BJ106KD	
	Inductor	L_{VDD2}	1 μH	Range ± 30% DCR maximum = 100 mΩ	
VIO	Capacitor	$C_{VIO.IN}$	10 μF	Range ± 50% ESR minimum = 1 mΩ ESR maximum = 20 mΩ Taiyo Yuden: JMK212BJ106KD	Figure 4-1
	Capacitor	$C_{VIO.OUT}$	10 μF	Range ± 50% ESR minimum = 1 mΩ ESR maximum = 20 mΩ Taiyo Yuden: JMK212BJ106KD	
	Inductor	L_{VVIO}	1 μH	Range ± 30% DCR maximum = 100 mΩ	
VRUSB_3V	Capacitor	$C_{VUSB.3P1}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 300 mΩ	Figure 4-1 Figure 7-2
VRUSB_1V5	Capacitor	$C_{VINTUSB1P5.OUT}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1 Figure 7-2
VRUSB_1V8	Capacitor	$C_{VINTUSB1P8.OUT}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1 Figure 7-2
VDAC	Capacitor	$C_{VDAC.IN}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
	Capacitor	$C_{VDAC.OUT}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	
VPLLA3R	Capacitor	$C_{VPLLA3R.IN}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VPLL1	Capacitor	$C_{VPLL1.OUT}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VPLL2/VDSI.CSI	Capacitor	$C_{VPLL2.OUT}$	1 μF	Range: 0.3 to 2.7 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1

Table 15-1. TPS65950 External Components (continued)

Function	Component	Reference	Value	Note	Link
VMMC1	Capacitor	$C_{VMMC1.IN}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
	Capacitor	$C_{VMMC1.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	
VMMC2	Capacitor	$C_{VMMC2.IN}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
	Capacitor	$C_{VMMC2.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	
VSIM	Capacitor	$C_{VSIM.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VAUX12S	Capacitor	$C_{VAUX12S.IN}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VAUX1	Capacitor	$C_{VAUX1.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VAUX2	Capacitor	$C_{VAUX2.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VAUX3	Capacitor	$C_{VAUX3.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VAUX4	Capacitor	$C_{VAUX4.IN}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
	Capacitor	$C_{VAUX4.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	
VINT	Capacitor	$C_{VINT.IN}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VINTANA1	Capacitor	$C_{VINTANA1.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VINTANA2	Capacitor	$C_{VINTANA2.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VINTDIG	Capacitor	$C_{VINTDIG.OUT}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 4-1
VBAT.USB	Capacitor	$C_{VBAT.USB}$	1 µF	Range: 0.3 to 2.7 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	Figure 7-2
USB CP	Capacitor	$C_{VBUS.FC}$	2.2 µF ±40%	ESR maximum = 20 mΩ	Figure 7-2
	Capacitor	$C_{VBUS.IN}$	10 µF		
	Capacitor	C_{VBUS}	4.7 µF ±40%	ESR maximum = 20 mΩ	

Table 15-1. TPS65950 External Components (continued)

Function	Component	Reference	Value	Note	Link
MCPC					
	Capacitor	C_{TXAF}	0.1 µF		Figure 7-2
	Capacitor	C_{RXAF}	1 µF		
	Resistor	R_{RTSO}	22 Ω/100 Ω		
	Diode	D_{CTSI1}		NNCD5.6J	
	Diode	D_{CTSI2}		NNCD5.6J	
	Diode	D_{RTSO1}		NNCD5.6J	
	Diode	D_{RTSO2}		NNCD5.6J	
32.768 kHz					
	Capacitor	C_{XIN}	10 pF	Range: 9 to 12.5 pF	Figure 12-5
	Capacitor	C_{XOUT}	10 pF		
	Quartz	$X_{32.768kHz}$	32.768 kHz	±30 ppm (at 25°C) ±200 ppm (–40°C to 85°C)	
Audio					
Earpiece	Capacitor	C_{EAR}	100 pF		Figure 6-3
8-Ω hands-free right	Ferrite bead	$L_{HFR.M}$		NEC: N2012ZPS121	Figure 6-5
	Ferrite bead	$L_{HFR.P}$		NEC: N2012ZPS121	
	Capacitor	C_{HFR}	1 µF		
	Capacitor	$C_{HFR.M}$	1 nF		
	Capacitor	$C_{HFR.P}$	1 nF		
8-Ω hands-free left	Ferrite bead	$L_{HFL.M}$		NEC: N2012ZPS121	Figure 6-5
	Ferrite bead	$L_{HFL.P}$		NEC: N2012ZPS121	
	Capacitor	C_{HFL}	1 µF		
	Capacitor	$C_{HFL.M}$	1 nF		
	Capacitor	$C_{HFL.P}$	1 nF		
Headset left	Capacitor	C_S	22 µF/47 µF		Figure 6-7 through Figure 6-10
	Resistor	R_S	0 to 33 Ω		
	Capacitor	C_I	47 pF		
Headset right	Capacitor	C_S	22 µF/47 µF		Figure 6-7 through Figure 6-10
	Resistor	R_S	0 to 33 Ω		
	Capacitor	C_I	47 pF		
Headset microphone	Capacitor	$C_{HM.M}$	100 nF		Figure 6-7 through Figure 6-10
	Capacitor	$C_{HM.P}$	100 nF		
	Capacitor	$C_{HM.O}$	47 pF		
	Resistor	$R_B + R_{SB}$	2.2 kΩ/2.7 kΩ		
	Capacitor	C_B	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability.	
External class-D predriver left	Capacitor	$C_{PL.O}$	50 pF		Figure 6-12
	Capacitor	C_{PL}	1 µF		
	Resistor	R_{PL}	>15 kΩ		
	Resistor	$R_{PL.M}$	>15 kΩ		
	Resistor	$R_{PL.O}$	10 kΩ		
	Capacitor	$C_{PL.M}$	1 µF		

Table 15-1. TPS65950 External Components (continued)

Function	Component	Reference	Value	Note	Link
External class-D predriver right	Capacitor	$C_{PR.O}$	50 pF		Figure 6-12
	Capacitor	C_{PR}	1 μF		
	Resistor	R_{PR}	>15 kΩ		
	Resistor	$R_{PR.M}$	>15 kΩ		
	Resistor	$R_{PR.O}$	10 kΩ		
	Capacitor	$C_{PR.M}$	1 μF		
Vibrator H-bridge	Ferrite bead	$L_{V.M}$		BLM18BD221S1N	Figure 6-13
	Ferrite bead	$L_{V.P}$		BLM18BD221S1N	
	Capacitor	$C_{V.V}$	1 μF		
	Capacitor	$C_{V.M}$	1 nF		
	Capacitor	$C_{V.P}$	1 nF		
Main microphone (pseudodifferential mode)	Capacitor	$C_{MM.M}$	100 nF		Figure 6-20
	Capacitor	$C_{MM.P}$	100 nF		
	Capacitor	$C_{MM.O}$	47 pF		
	Resistor	$R_{MM.O}$	~500 Ω		
	Resistor	$R_{MM.MP}$	~1.7 kΩ		
	Capacitor	$C_{MM.B}$	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability.	
Submicrophone (pseudodifferential mode)	Capacitor	$C_{MS.M}$	100 nF		Figure 6-20
	Capacitor	$C_{MS.P}$	100 nF		
	Capacitor	$C_{MS.O}$	47 pF		
	Resistor	$R_{MS.O}$	~500 Ω		
	Resistor	$R_{MS.MP}$	~1.7 kΩ		
	Capacitor	$C_{MS.B}$	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability.	
Main microphone (differential mode)	Capacitor	$C_{MM.M}$	100 nF		Figure 6-21
	Capacitor	$C_{MM.P}$	100 nF		
	Capacitor	$C_{MM.PM}$	47 pF		
	Capacitor	$C_{MM.O}$	47 pF		
	Capacitor	$C_{MM.GM}$	47 pF		
	Capacitor	$C_{MM.GP}$	47 pF		
	Resistor	$R_{MM.BP}$	1 kΩ		
	Resistor	$R_{MM.GM}$	1 kΩ		
	Capacitor	$C_{MM.B}$	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability.	
Submicrophone (differential mode)	Capacitor	$C_{MS.M}$	100 nF		Figure 6-21
	Capacitor	$C_{MS.P}$	100 nF		
	Capacitor	$C_{MS.PM}$	47 pF		
	Capacitor	$C_{MS.O}$	47 pF		
	Capacitor	$C_{MS.GM}$	47 pF		
	Capacitor	$C_{MS.GP}$	47 pF		
	Resistor	$R_{MS.BP}$	1 kΩ		
	Resistor	$R_{MS.GM}$	1 kΩ		
	Capacitor	$C_{MS.B}$	0 to 200 pF	If greater than 200 pF, a serial resistor is required for bias stability.	
VMIC1	Capacitor	$C_{VMIC1.OUT}$	1 μF	Range: 0.3 to 3.3 μF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	

Table 15-1. TPS65950 External Components (continued)

Function	Component	Reference	Value	Note	Link
VMIC2	Capacitor	$C_{VMIC2.OUT}$	1 µF	Range: 0.3 to 3.3 µF ESR minimum = 20 mΩ ESR maximum = 600 mΩ	
Silicon microphone	Capacitor	C_{SM}	1 µF		Figure 6-24
	Capacitor	$C_{SM.P}$	100 nF		
	Capacitor	$C_{SM.M}$	100 nF		
	Capacitor	$C_{SM.PG}$	47 nF		
	Resistor	R_{SM}	>500 Ω		
Auxiliary left	Capacitor	C_{AUXL}	100 nF		Figure 6-25
	Capacitor	$C_{AUXL.M}$	47 pF		
Auxiliary right	Capacitor	C_{AUXR}	100 nF		
	Capacitor	$C_{AUXR.M}$	47 pF		
LED Driver					
	Resistor	$R_{LED.A}$	120 Ω	Requirerd for each LED	Figure 10-1
	Resistor	$R_{LED.B}$	160 kΩ	Requirerd for each LED	
Battery Charger					
ICTLAC1	Capacitor	C_{COMPAC}	100 nF		Figure 8-1 Figure 8-2
	Resistor	$R_{SCOMPAC}$	51 Ω		Figure 8-1 Figure 8-2
	FET	T_{AC}	FDJ1027P	Fairchild	Figure 8-1 Figure 8-2
	Resistor	$R_{LimitAC}$	700 kΩ		Figure 8-1 Figure 8-2
	FET	T_3	FDY100PZ		Figure 8-2
	Capacitor	C_3	1 nF		Figure 8-2
	Resistor	R_3	100 kΩ		Figure 8-2
ICTLUSB1	Capacitor	$C_{COMPUSB}$	100 nF		Figure 8-1
	Resistor	$R_{SCOMPUSB}$	51 Ω		
	FET	T_{USB}	FDJ1027P	Fairchild	
	Resistor	$R_{LimitUSB}$	500 kΩ		
VPRECH	Capacitor	C_{PRECH}	1 µF		Figure 8-1
VCCS	Resistor	R_S	220 mΩ		Figure 8-1
BCI AUTO	Resistor	$R_{BCI.AUTO}$	<10 kΩ >140 kΩ	For more information, see Table 8-2.	Figure 8-3
VBAT	Capacitor	C_{CV}	80 µF		Figure 8-1
I^2C Bus—External Pullup					
I^2C SmartReflex	Resistor	$R_{PSR.SDA}$		Pullups for various bus capacitances (C_L) and I^2C speeds (standard, fast, and HS) If C_L = 10 pF: Standard = 118 kΩ, Fast = 35.4 kΩ, HS = 4.7 kΩ If C_L = 12 pF: Standard = 98.3 kΩ, Fast = 29.5 kΩ, HS = 3.9 kΩ If C_L = 50 pF: Standard = 23.6 kΩ, Fast = 7.1 kΩ, HS = 940 Ω If C_L = 100 pF: Standard = 11.8 kΩ, Fast = 3.54 kΩ, HS = 470 Ω If $C_L \leq$ 12 pF, there is no need for an external pullup; the internal 3-kΩ pullup can be used. If an external pullup is used, disable the internal 3-kΩ pullup (reference the GPPUPDCTR1 register; see the TRM).	Section 13.3
	Resistor	$R_{PSR.SCL}$			
I^2C control	Resistor	R			
	Resistor	$R_{CNTL.SCL}$			

16 TPS65950 Package

16.1 TPS65950 Standard Package Symbols

Table 15-1 shows the TPS65950 printed device reference.

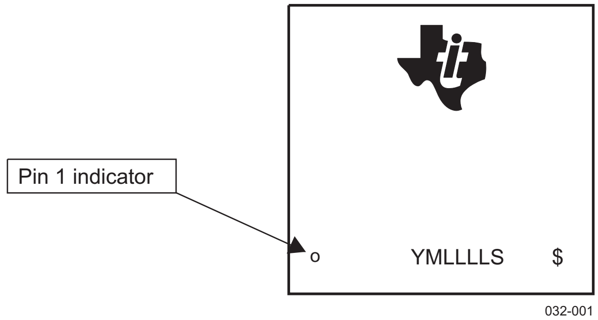


Figure 16-1. Printed Device Reference

Table 16-1 lists the symbols used in the TPS65950 nomenclature.

Table 16-1. TPS65950 Nomenclature Description

Field	Meaning
P	Prototype (X), preproduction (P), or qualified/production device (blank)(1)
A	Mask set version descriptor (initial silicon = blank, first silicon revision = A, second silicon revision = B,...)(2)
YM	Year month
LLLLS	Lot code
$	Fab planning code

(1) A blank in the symbol or part number is collapsed so there are no gaps between characters.
(2) Initial silicon version is ES1.0; first revision can be named ES2.0, ES1.1 or ES1.01, depending on the level of change.
Note: Device name is a maximum of 10 characters.

16.2 Package Thermal Resistance Characteristics

Table 16-2 lists the thermal resistance characteristics for the recommended package types used for the TPS65950.

Table 16-2. TPS65950 Thermal Resistance Characteristics

Package	$R_{\theta JA}$(°C/W)	$R_{\theta JB}$(°C/W)	$R_{\theta JC}$(°C/W)	Board Type
TPS65950	38.4	15.2	19.2(1)	1S2P(2)
TPS65950	56.5	15.5	19.2(1)	1S0P(2)

(1) Not applicable. Because the POP package has a memory package on top, no heat sink can be used.
(2) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, Test Board for Area Array Surface Mount Package Thermal Measurements).

16.3 Mechanical Data

Figure 16-2 is the top view of the TPS65950 mechanical package.

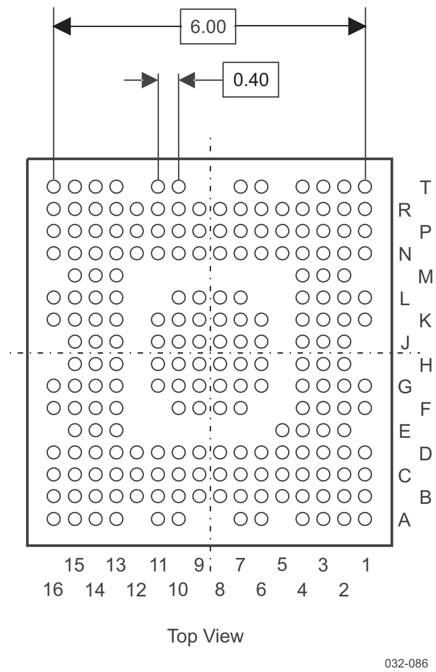


Figure 16-2. TPS65950 Mechanical Package Top View

Figure 16-3 shows the ball size.

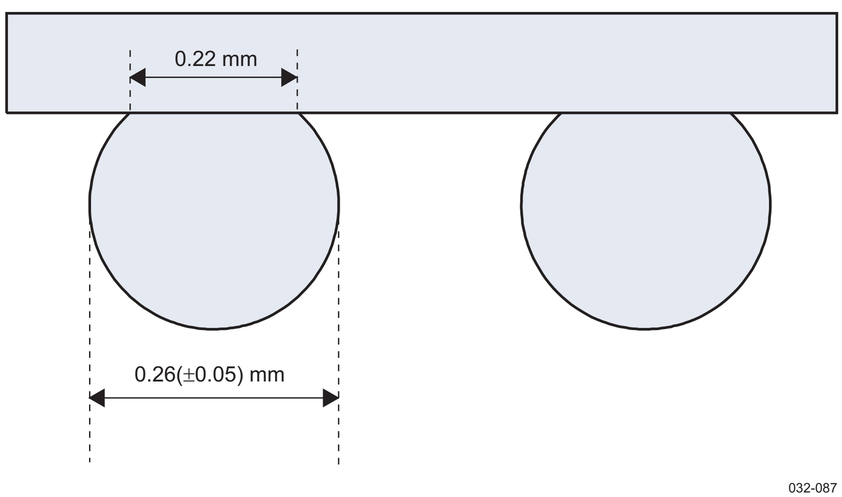


Figure 16-3. Ball Size

16.4 ESD Specifications

The device has built-in ESD protection to the limits specified below. It is recommended that the leads are shorted together, or the device placed in conductive foam, during storage or handling to prevent electrostatic damage.

ESD Method	Standard Reference	Performance
Human Body Model (HBM)	EIA / JESD22-A114D	1000V for internal pins 2000V for external pins (1)
Charge Device Model (CDM)	EIA / JESD22-C101C	500V

(1) List of external pins: VAC, VBUS, DP/UART3.RXD, DN/UART3.TXD, ID, VPLL1.OUT, VMMC1.OUT, VMMC2.OUT, VSIM.OUT.

17 Glossary

ADC	Analog-to-digital converter
ALC	Automatic level control
ARIB	Association of Radio Industries and Businesses
ASIC	Application-specific integrated circuit
BCI	Battery charger interface
BGA	Ball grid array
BT	Bluetooth
BW	Signal bandwidth
CMOS	Complementary metal oxide semiconductor
Codec	Coder/decoder
CMT	Cellular mobile telephone
CPU	Central processing unit
DAC	Digital-to-analog converter
DBB	Digital baseband
DCR	Direct current (dc) resistance
DM	Data manual
DSP	Digital signal processor
DVFS	Dynamic voltage and frequency scaling
ESD	Electrostatic discharge
ESR	Equivalent series resistance
FET	Field effect transistor
FSR	Full-scale range
GP	General-purpose
GPIO	General-purpose input/output
hiZ	High impedance
HS	High speed or high security
HW	Hardware
I^2C	Inter-integrated circuit
I2S	Inter-IC sound
IC	Integrated circuit
ICN	Idle channel noise
ID	Identification
IDDQ	Direct drain quiescent current
IF	Interface
IO or I/O	Input/output
JTAG	Joint Test Action Group, IEEE 1149.1 standard
LED	Light emitting diode
LDO	Low-dropout regulator
LJF	Left-justified format

LS	Low speed
MADC	Monitoring analog-to-digital converter
MCPC	Mobile Computing Promotion Consortium
MEMS	Micro-electrical-mechanical system
NA, N/A	Not applicable
NRZI	Nonreturn to zero inverted
OCP	Open-core protocol
OTG	On-the-go
PBGA	Plastic ball grid array
PCB	Printed circuit board
PCM	Pulse-code modulation
PD	Pulldown
PDM	Pulse density modulated
PFM	Pulse frequency modulation
PLL	Phase-locked loop
PMOS	Portable media operating system
POL	Polarity
POR	Power-on reset
PSRR	Power supply ripple rejection
PU	Pullup
PWL	Pulse-width length
PWT	Pulse-width time
PWM	Pulse-width modulation
RFID	Radio frequency identification
RJF	Right-justified format
RTC	Real-time clock
RX	Receive
SDI	Serial display Interface
SMPS	Switch-mode power supply
SNR	Signal-to-noise ratio
SRP	Secure remote password
SW	Software
SYNC/SYNCHRO	Synchronization
SYS	System
TAP	Test access port
TBD	To be defined
TDM	Time division multiplexing
THRU	Feed through
TRM	Technical reference manual
TX	Transmit

UART	Universal asynchronous receiver/transmitter
ULPI	UTMI+ low pin interface
UPR	Uninterrupted power rail
USB	Universal serial bus
UTMI	USB transceiver macrocell interface

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS65950A2ZXN	ACTIVE	NFBGA	ZXN	209	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65950A2ZXNR	ACTIVE	NFBGA	ZXN	209	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65950A3ZXN	ACTIVE	NFBGA	ZXN	209	260	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65950A3ZXNR	ACTIVE	NFBGA	ZXN	209	2000	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR	
TPS65950BZXN	OBSOLETE	NFBGA	ZXN	209		TBD	Call TI	Call TI	
TPS65950BZXNR	OBSOLETE	NFBGA	ZXN	209		TBD	Call TI	Call TI	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

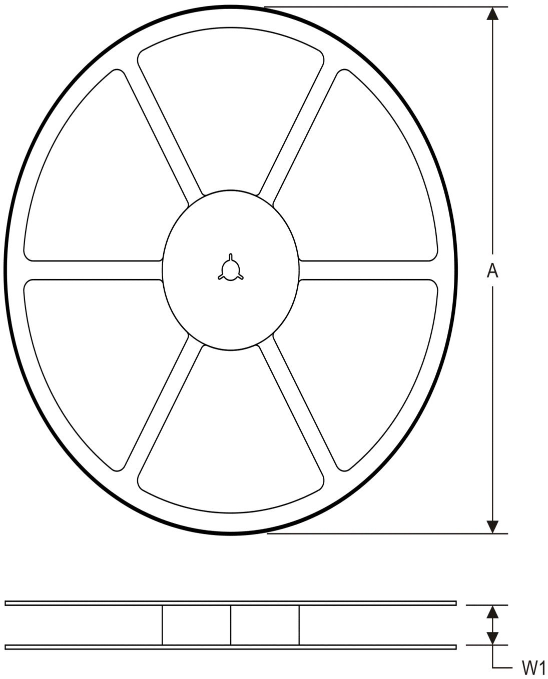
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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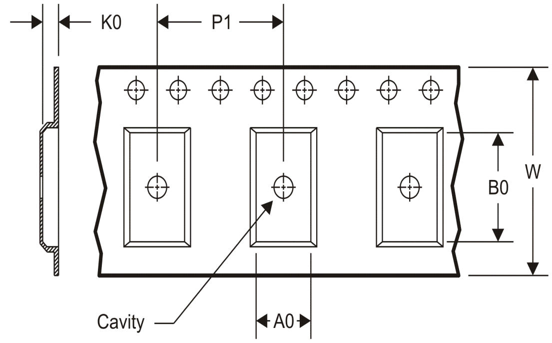
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



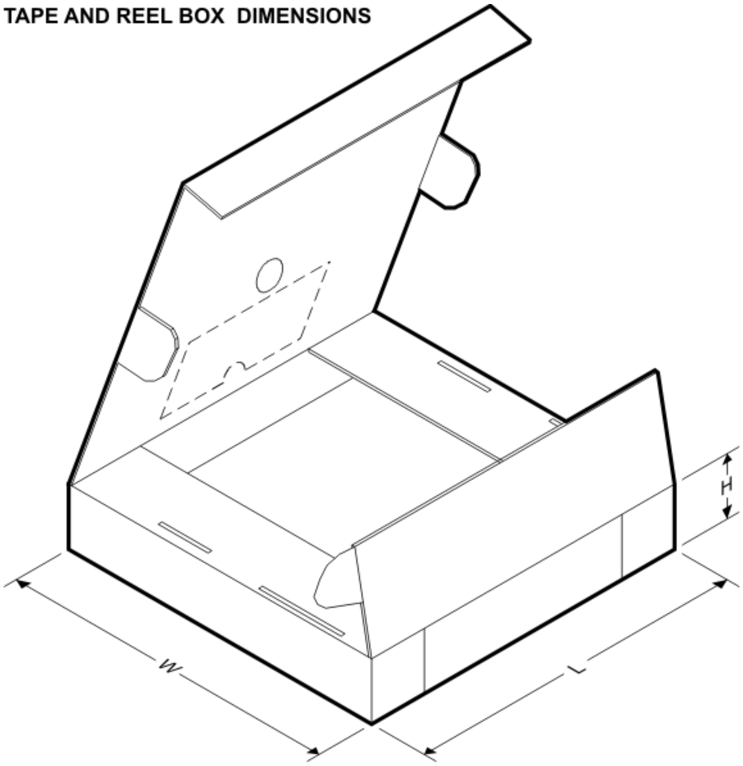
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65950A2ZXNR	NFBGA	ZXN	209	2000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
TPS65950A3ZXNR	NFBGA	ZXN	209	2000	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

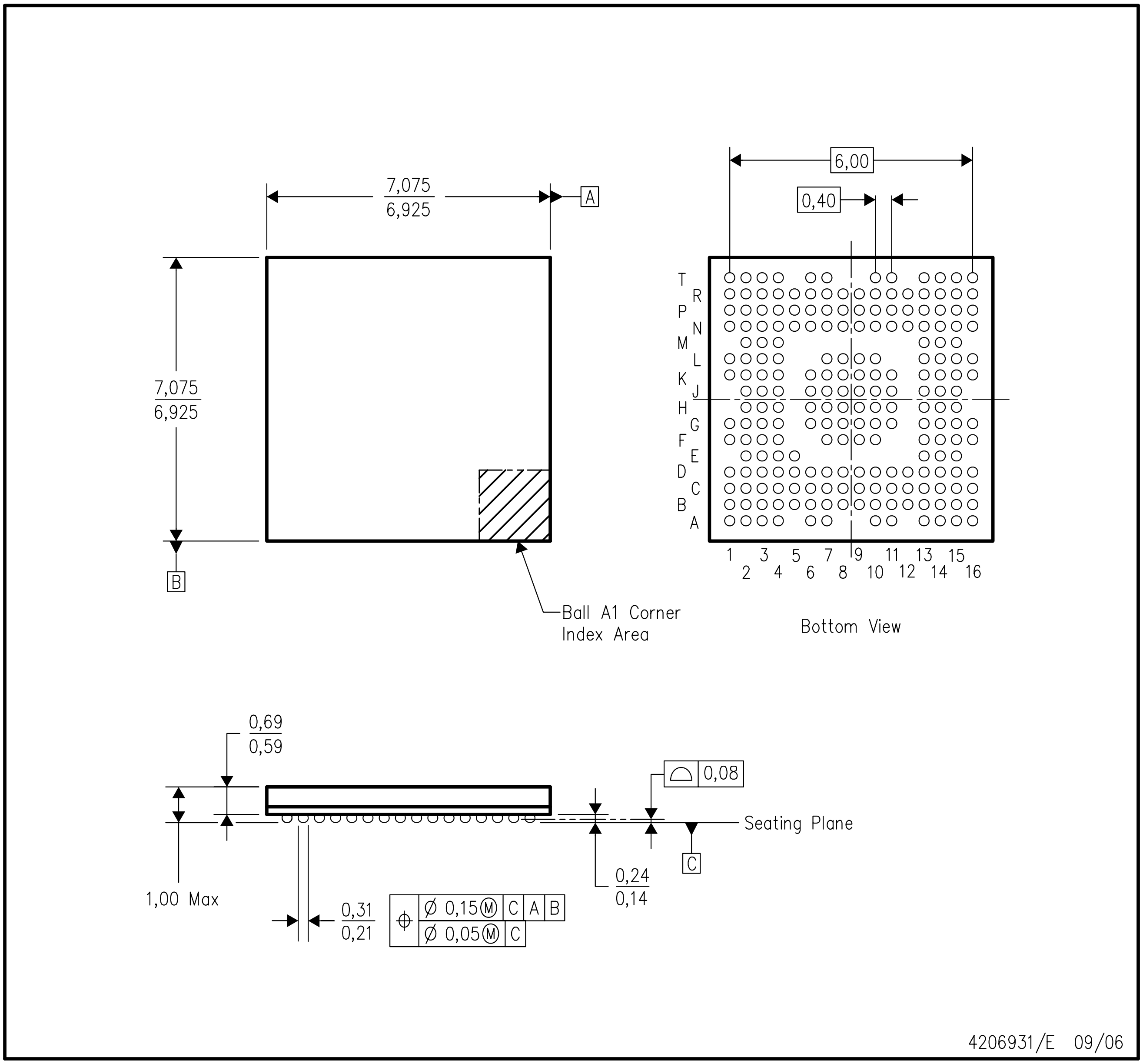
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65950A2ZXNR	NFBGA	ZXN	209	2000	336.6	336.6	31.8
TPS65950A3ZXNR	NFBGA	ZXN	209	2000	336.6	336.6	31.8

ZXN (S-PBGA-N209) PLASTIC BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.